



LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

O2Micro OZ8681

System Charge Power (+BATCHG)

P2806
System Discharge Power
(+1.5V/+3V/+5V)

Ricktek RT8205
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

NCP6132/NCP5911/RT8209/G9334
Processor Power (+VCC_CORE/
+1.05_VTT/+VCCSA)

Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)


Richtek RT8209/RT9025
PCH Power (+1.05/+1.8V)

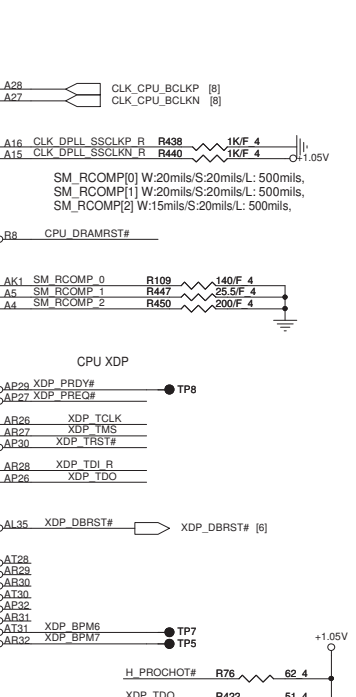
O2Micro OZ8122
DGPU Power (+VGACORE/+3.3V_GFX/
+1.8_VGA/+1.5_GFX/+1.05_GFX)



PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size A3	Document Number Block Diagram	Rev A
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 NB5	Size	Document Number	
	Custom	Processor 1/4 (Host/GPU)	
	Date:	Tuesday, March 27, 2012	Sheet 2 of 2



SM_DRAMPWROK
Processor Input.

3

DDR3 DRAM RESET

Q15
ME2N7002D

3,12,13] DRAMRST_CNTRL_PCH

C338
0.047µ/10V 4



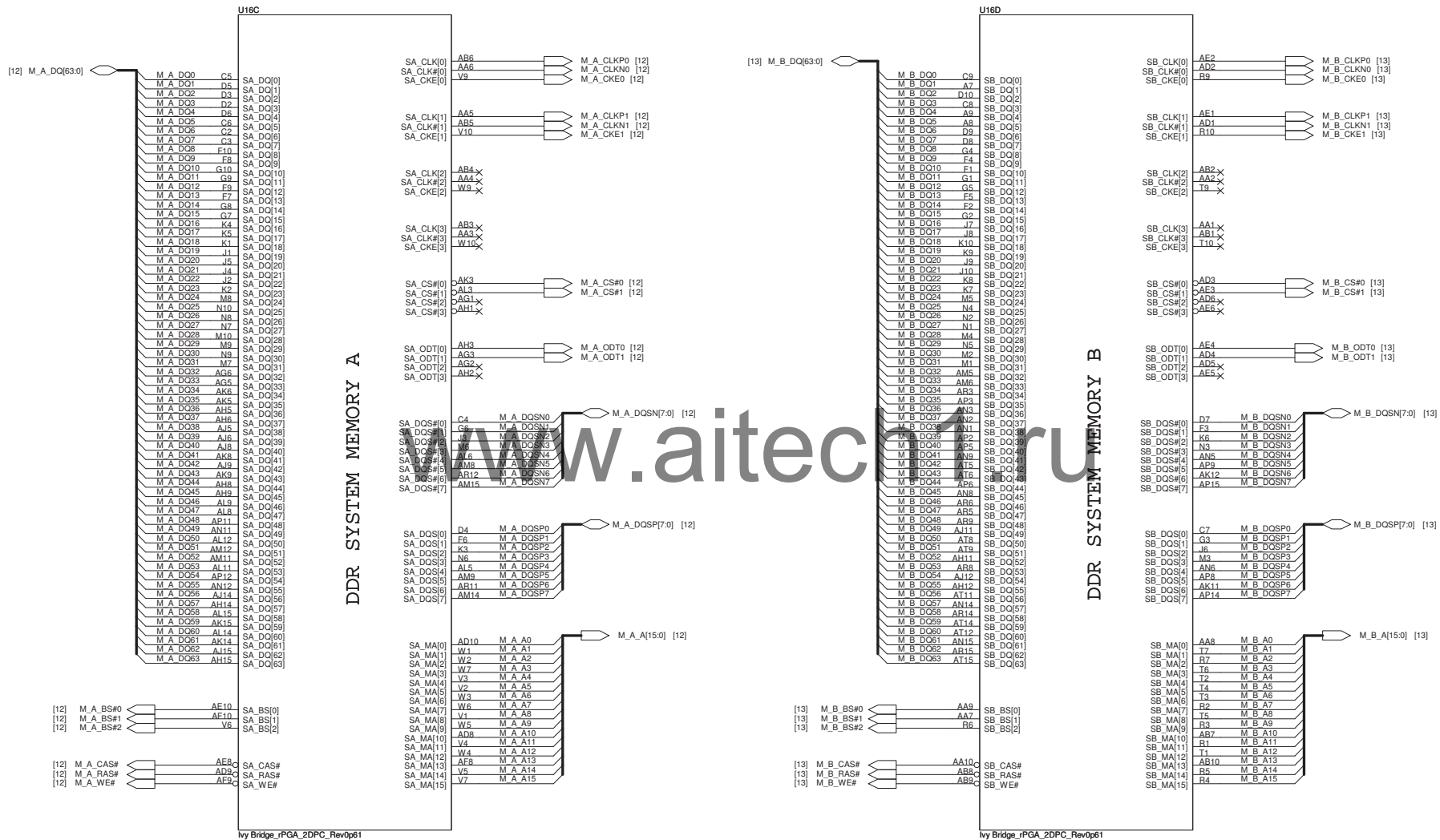


NB5

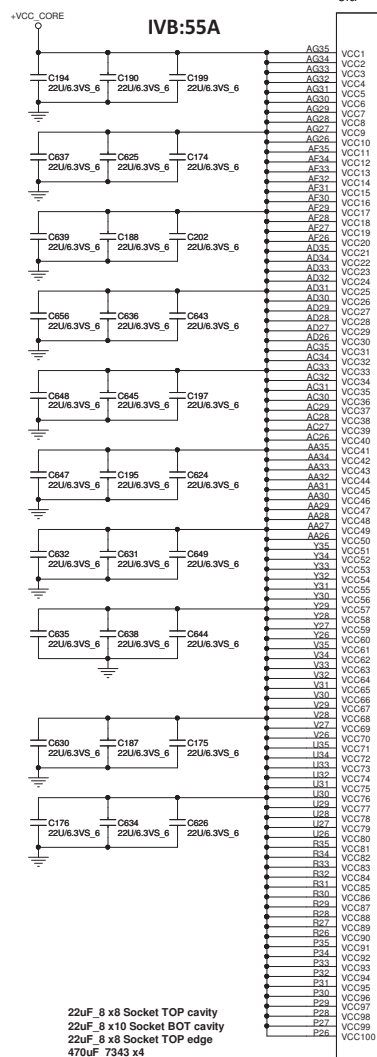
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number Processor 1/4 (Host/GPU)	Rev A
Date: Tuesday, March 27, 2012	Sheet	2 of 42

Ivy Bridge Processor (DDR3)



POWER

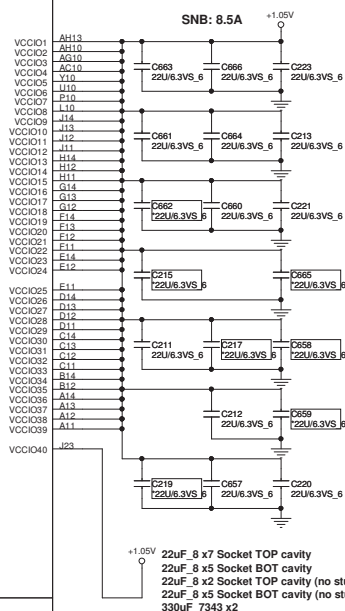
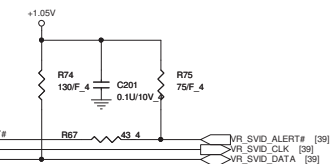


by Bridge_rPGA_2DPC_Rev0p1

CORE SUPPLY

SVID

SENSE LINES



100- ±1% pull-up to VCC near processor.

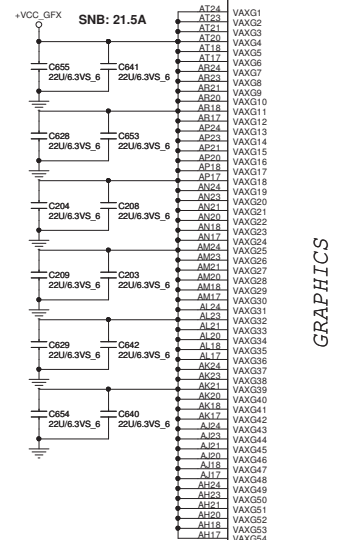
R91,R98,R109 close to CPU

Zo impedance: 27.4ohm

Zo impedance: 27.4ohm

POWER

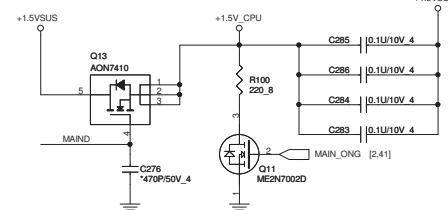
CAD Note: +VDDR_REF_CPU should have 10 mil trace width



GRAPHICS

1.8V RAIL

by Bridge_rPGA_2DPC_Rev0p1



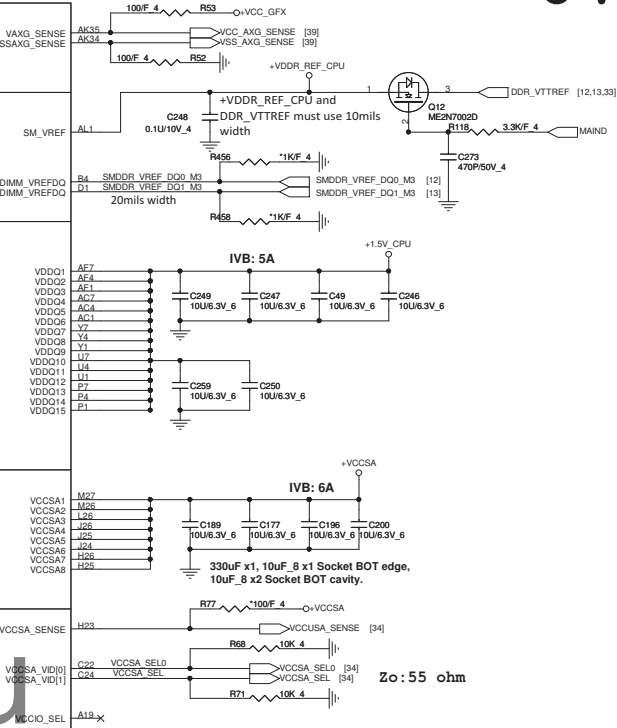
SENSE LINES

VREF

DDR3 -1.5V RAILS

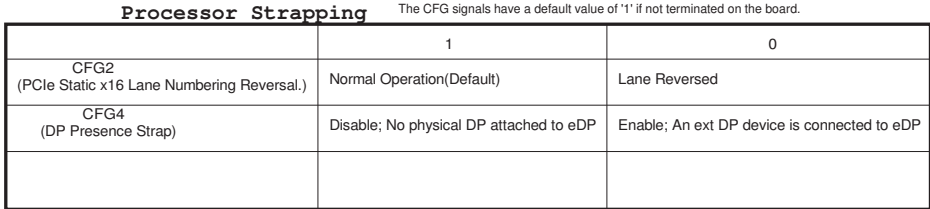
SA RAIL


MISC

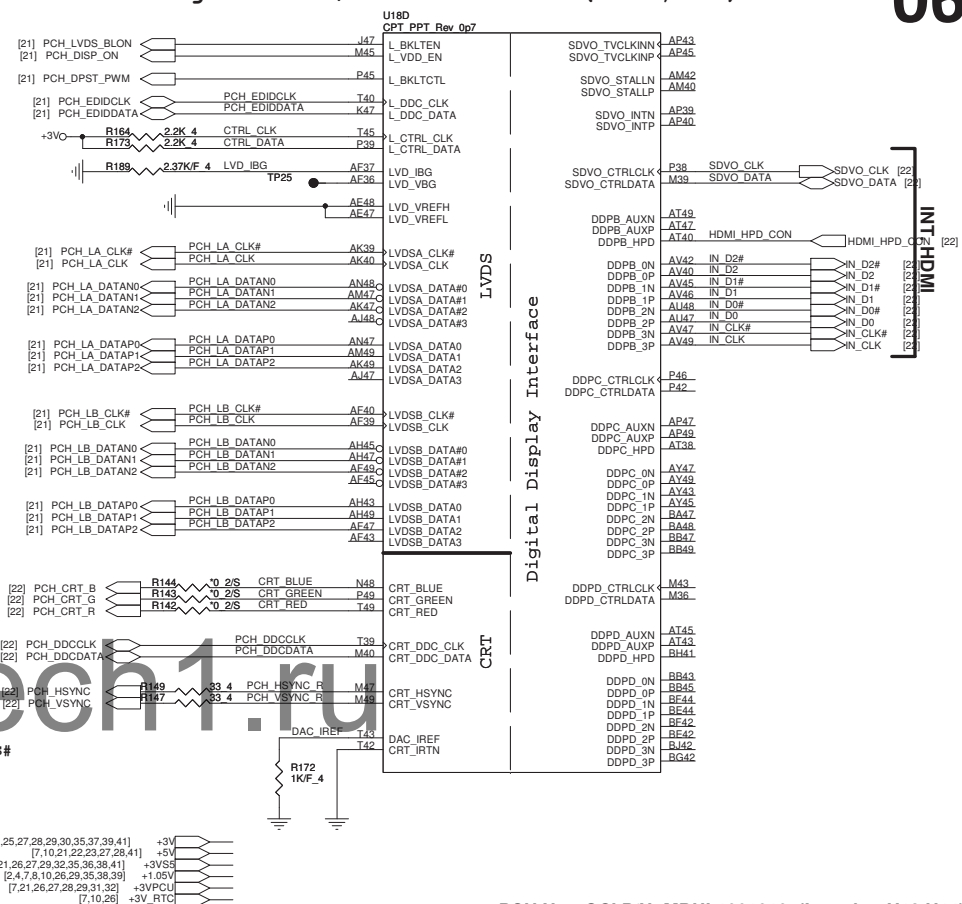


PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom Document Number Processor 3/4 (POWER)
Date: Tuesday, March 27, 2012 Sheet 4 of 42

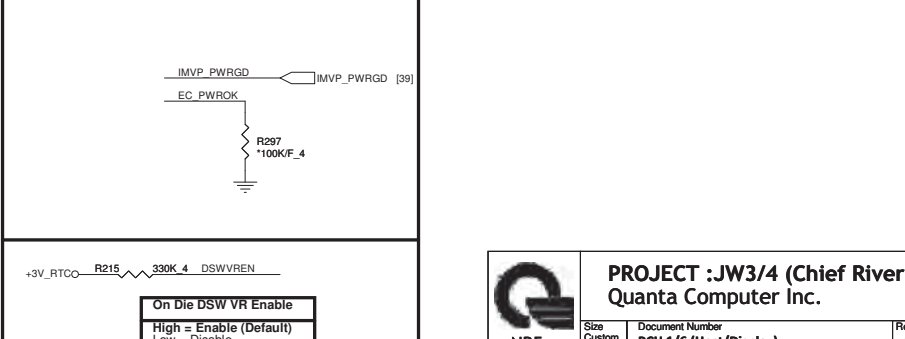
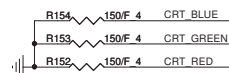


 NB5	PROJECT :JW3/4 (Chief River) Quanta Computer Inc.		
	Size Custom	Document Number Processor 4/4 (RSV,Ground)	Rev A
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PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

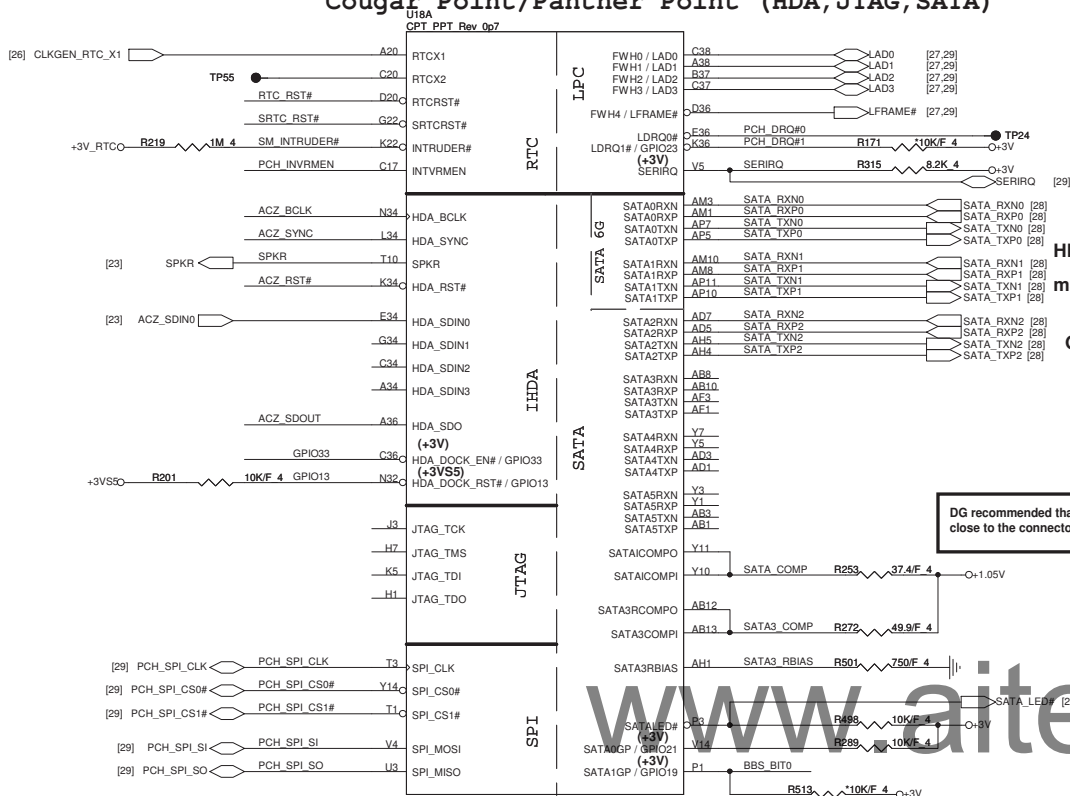
System PWR_OK(CLG)



PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number PCH 1/6 (Host/Display)	Rev A
Date: Tuesday, March 27, 2012	Sheet 6 of	42

Cougar Point/Panther Point (HDA, JTAG, SATA)



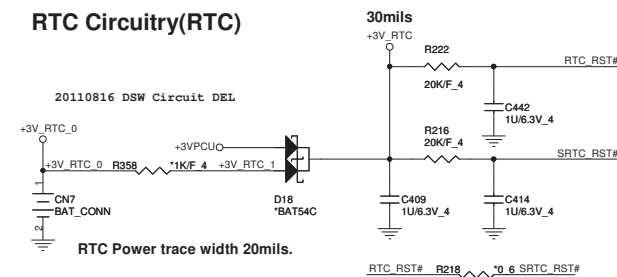
HDD0 (SATA3 6.0Gb/s)

mSATA (SATA4 3Gb/s)

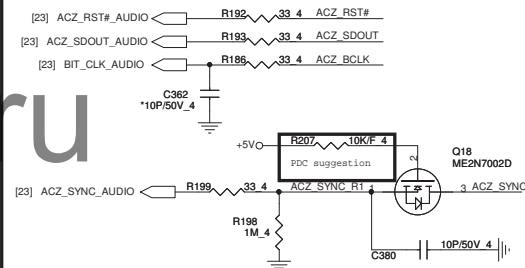
ODD (SATA2 3Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

RTC Circuitry(RTC)

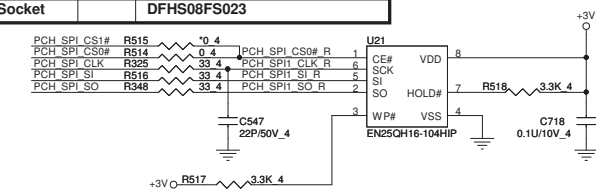


HDA Bus(CLG)



Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DFHS08FS023

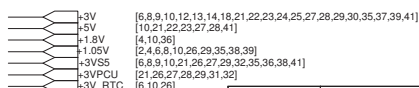
PCH SPI ROM(CLG)



PCH Strap Table

On-Chip Table

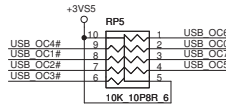
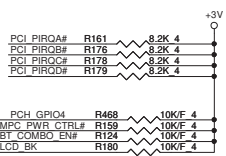
Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>0</td><td>0</td><td>SPI LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	0	0	SPI LPC	<div>Need external pull-down for LPC BIOS</div> <div>Default weak pull-up on GNT0/1#</div>
GNT1#	GNT0#	Boot Location								
0	0	SPI LPC								
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK								
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm							
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V							
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							



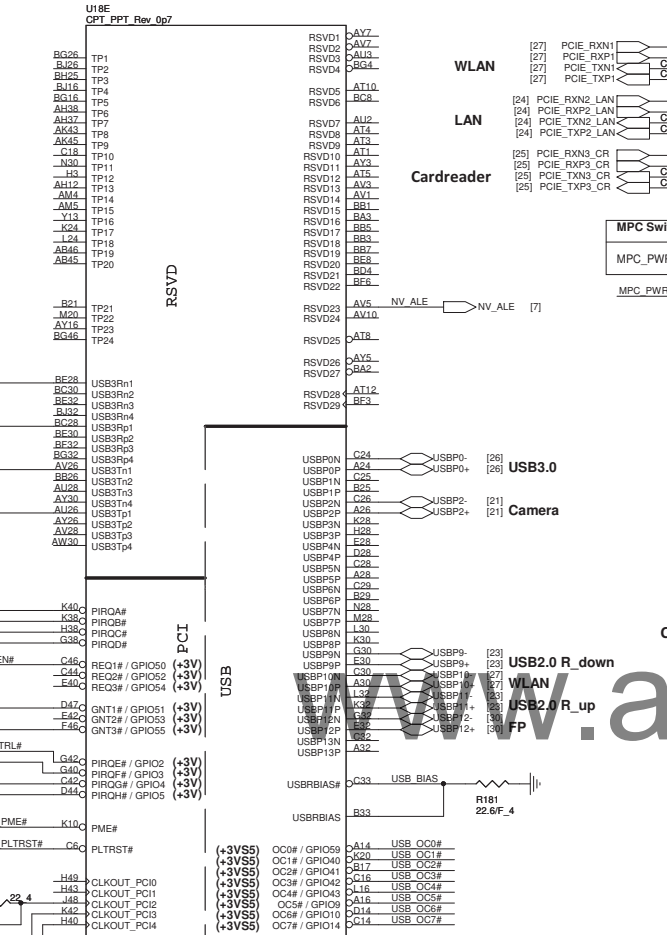
PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number	Rev A
Date: Tuesday, March 27, 2012	PCH 2/6 (HDA/RTC/SATA/SPI)	7 of 42

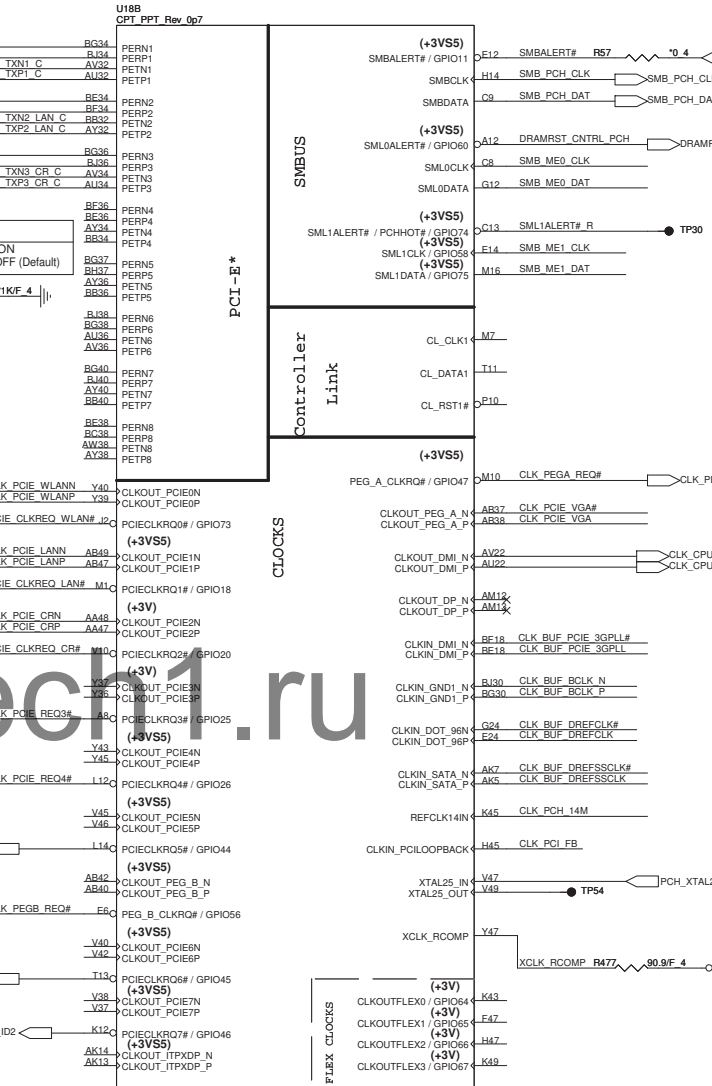
PCI/USB0C# Pull-up(CLG)



Cougar Point-M/Panther Point (PCI,USB,NVRAM)



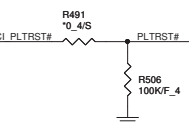
Cougar Point-M/Panther Point (PCI-E, SMBUS, CLK)



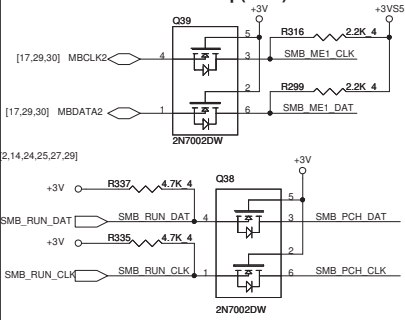
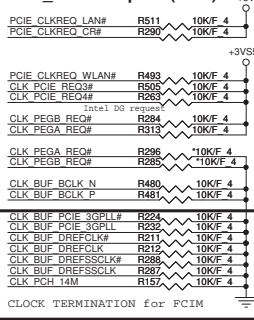
USB3.0

130 Modify USB3.0 for HM70

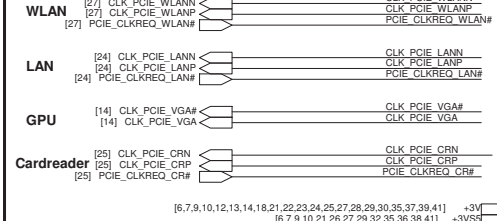
PLTRST#(CLG)



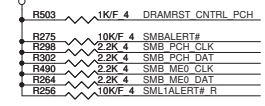
SMBus/Pull-up(CLG)

**CLK REQ/Strap Pin(0)**

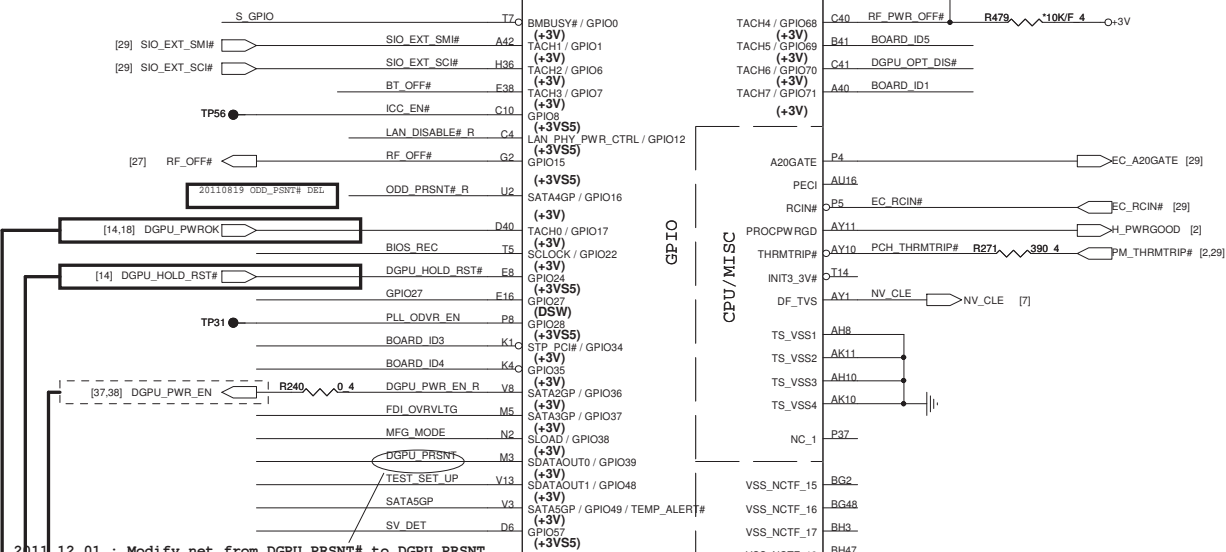
PCIE Clock



SMBus/Pull-up(CLG)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

U18F
CPT PPT Rev 0p7

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

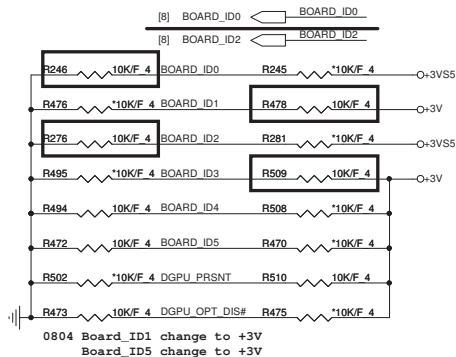
BOARD_ID[3:0] Model Name

0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3

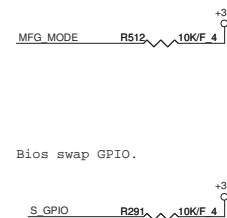
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	HM76=0, HM70=1
DGPU_PRST	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

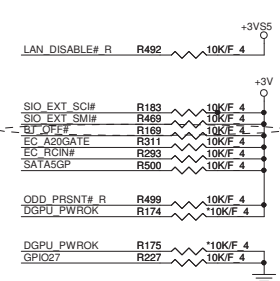
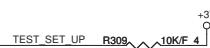
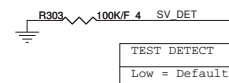
20110816 Define BRD_ID[3:0]

0804 Board_ID1 change to +3V
Board_ID5 change to +3V

MFG-TEST



GPIO Pull-up/Pull-down(CLG)

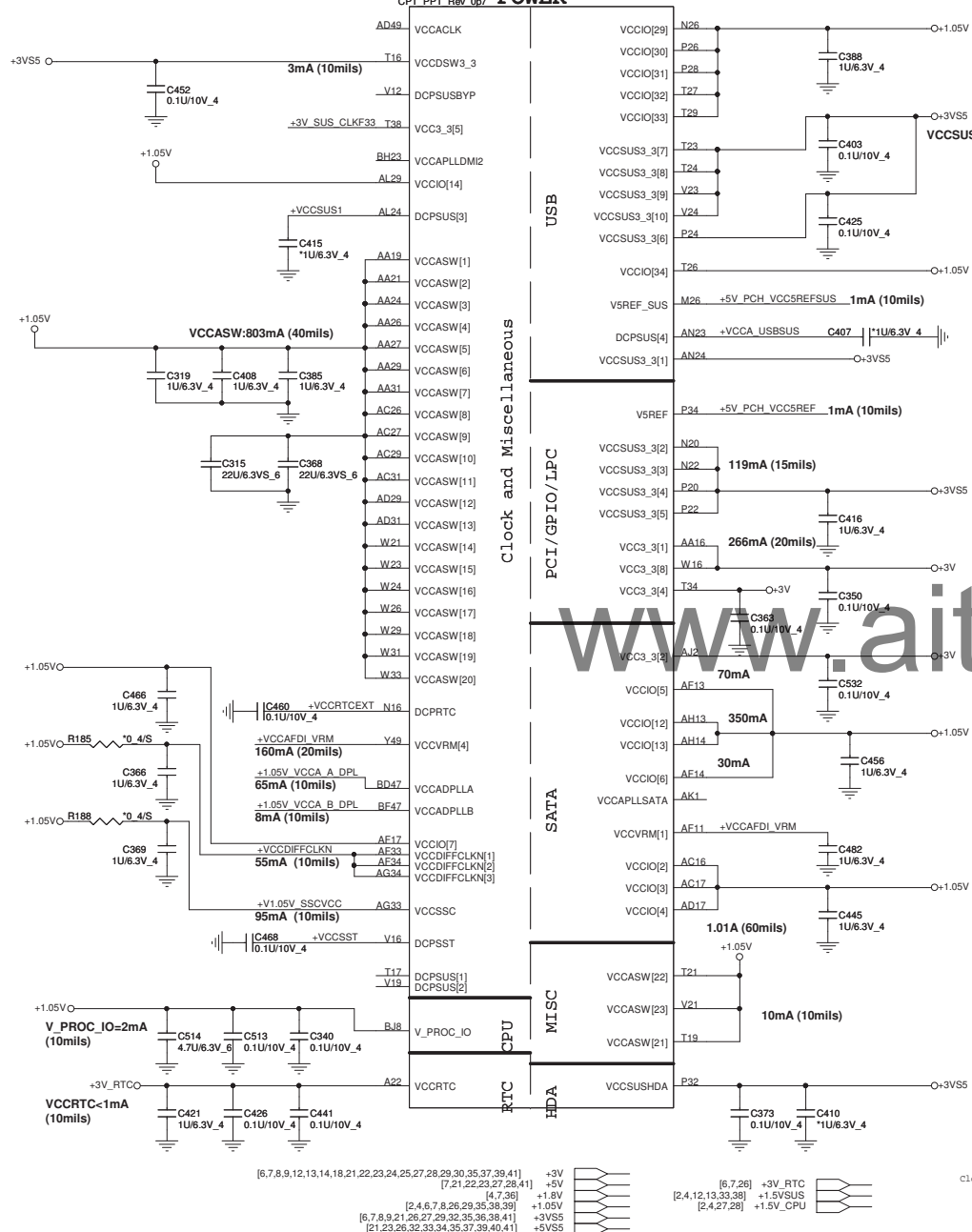
Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = EnableBIOS RECOVERY High = Disable (Default)
Low = EnableSV_SET_UP
High = Strong (Default)TEST DETECT
Low = Default

SATA2GP/GPIO36 Reserved only

FDI TERMINATION
VOLTAGE OVERRIDE Reserved only[6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41]
[6,7,8,10,21,26,27,29,32,35,36,38,41]
+3V
+3VSSPROJECT :JW3/4 (Chief River)
Quanta Computer Inc.Size Custom Document Number PCH 4/6 (GPIO) Rev A
Date: Tuesday, March 27, 2012 Sheet 9 of 42

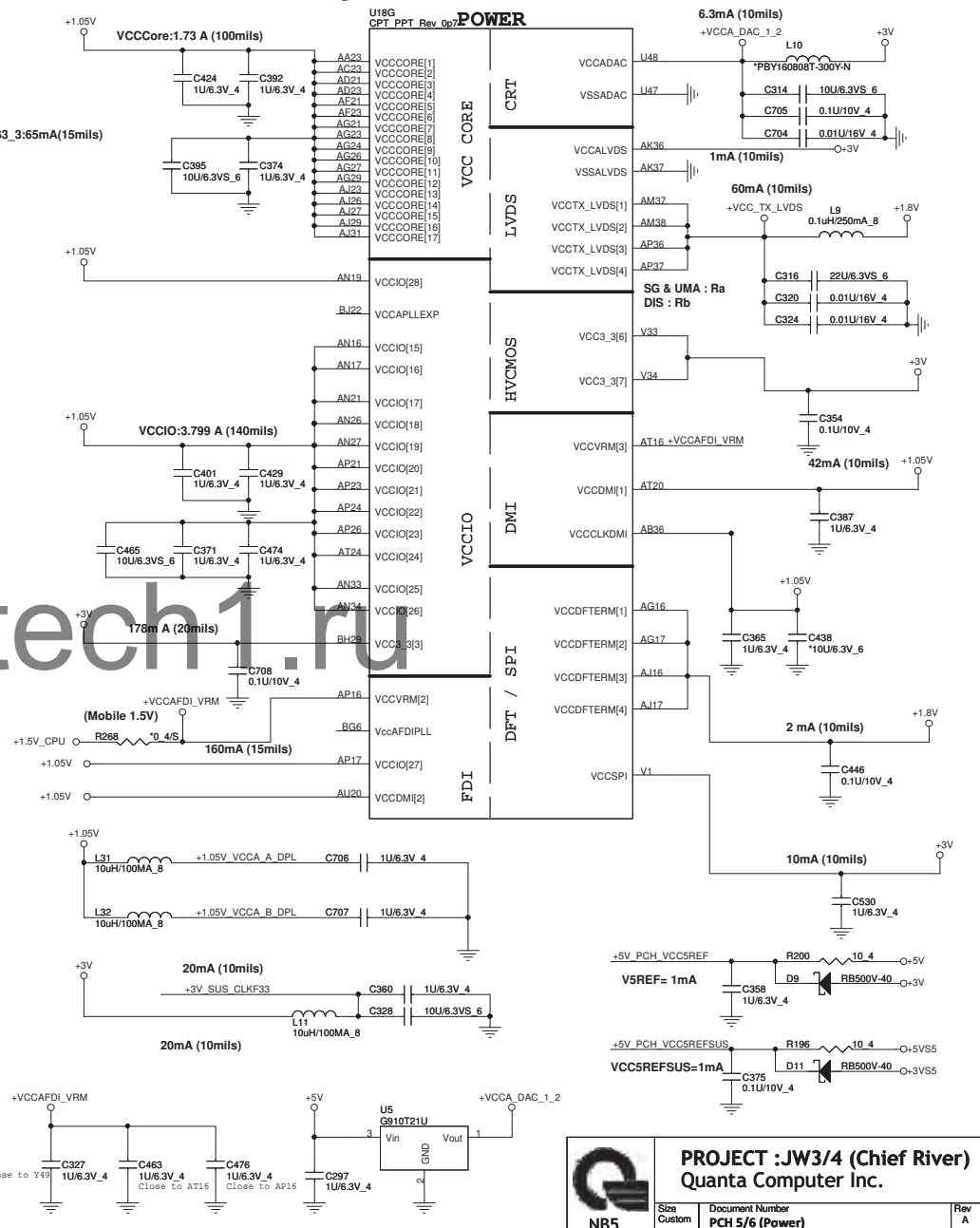
Cougar Point/Panther Point (POWER)

U18J
CPT PPT Rev 0p7 **POWER**



Cougar Point/Panther Point (POWER)

U18G
CPT PPT Rev 0n7



PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom	Document Number PCH 5/6 (Power)	Revision A
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Cougar Point/Panther Point (GND)

U18I
CPT_PPT_Rev_0p7

AY4	VSS[159]	H46	VSS[259]
AY42	VSS[160]	K18	VSS[260]
AY46	VSS[161]	K26	VSS[261]
AY8	VSS[162]	K39	VSS[262]
B11	VSS[163]	K46	VSS[263]
B15	VSS[164]	K7	VSS[264]
B19	VSS[165]	L18	VSS[265]
B23	VSS[166]	L2	VSS[266]
B27	VSS[167]	L20	VSS[267]
B31	VSS[168]	L26	VSS[268]
B35	VSS[169]	L28	VSS[269]
B39	VSS[170]	L36	VSS[270]
B7	VSS[171]	L48	VSS[271]
F45	VSS[172]	M12	VSS[272]
B812	VSS[173]	P16	VSS[273]
B816	VSS[174]	M18	VSS[274]
B820	VSS[175]	M22	VSS[275]
B822	VSS[176]	M24	VSS[276]
B824	VSS[177]	M30	VSS[277]
B826	VSS[178]	M32	VSS[278]
B830	VSS[179]	M34	VSS[279]
B838	VSS[180]	M38	VSS[280]
B84	VSS[181]	M4	VSS[281]
B846	VSS[182]	M42	VSS[282]
BC14	VSS[183]	M46	VSS[283]
BC18	VSS[184]	M6	VSS[284]
BC2	VSS[185]	N18	VSS[285]
BC22	VSS[186]	P30	VSS[286]
BC26	VSS[187]	N47	VSS[287]
BC32	VSS[188]	P11	VSS[288]
BC34	VSS[189]	P18	VSS[289]
BC36	VSS[190]	T33	VSS[290]
BC40	VSS[191]	P40	VSS[291]
BC42	VSS[192]	P43	VSS[292]
BC48	VSS[193]	P47	VSS[293]
BD46	VSS[194]	P7	VSS[294]
DD5	VSS[195]	P2	VSS[295]
BE22	VSS[196]	B48	VSS[296]
BE26	VSS[197]	T12	VSS[297]
BE40	VSS[198]	T31	VSS[298]
BE10	VSS[199]	T27	VSS[299]
BE12	VSS[200]	T4	VSS[300]
BE16	VSS[201]	W34	VSS[301]
BE20	VSS[202]	T46	VSS[302]
BE22	VSS[203]	T47	VSS[303]
BE24	VSS[204]	T8	VSS[304]
BE26	VSS[205]	V11	VSS[305]
BE28	VSS[206]	V26	VSS[306]
BD3	VSS[207]	V27	VSS[307]
BE30	VSS[208]	V29	VSS[308]
BE38	VSS[209]	V21	VSS[309]
BE40	VSS[210]	V36	VSS[310]
BF8	VSS[211]	V39	VSS[311]
BG17	VSS[212]	V43	VSS[312]
BG21	VSS[213]	V45	VSS[313]
BG33	VSS[214]	V47	VSS[314]
BG44	VSS[215]	W19	VSS[315]
BG8	VSS[216]	W2	VSS[316]
BH11	VSS[217]	W27	VSS[317]
BH15	VSS[218]	W48	VSS[318]
BH17	VSS[219]	Y12	VSS[319]
BH18	VSS[220]	Y4	VSS[320]
H10	VSS[221]	Y38	VSS[321]
BH27	VSS[222]	Y42	VSS[322]
BH31	VSS[223]	Y8	VSS[323]
BH33	VSS[224]	Y46	VSS[324]
BH35	VSS[225]	Y8	VSS[325]
BH39	VSS[226]	BG29	VSS[326]
BH43	VSS[227]	N24	VSS[327]
BH7	VSS[228]	A13	VSS[328]
D3	VSS[229]	AD47	VSS[329]
D12	VSS[230]	B43	VSS[330]
D16	VSS[231]	BE10	VSS[331]
D18	VSS[232]	BC41	VSS[332]
D22	VSS[233]	G14	VSS[333]
D24	VSS[234]	H16	VSS[334]
D26	VSS[235]	T36	VSS[335]
D30	VSS[236]	BG22	VSS[336]
D32	VSS[237]	BG24	VSS[337]
D34	VSS[238]	C22	VSS[338]
D38	VSS[239]	AP13	VSS[339]
D42	VSS[240]	M14	VSS[340]
D8	VSS[241]	AP3	VSS[341]
E18	VSS[242]	BE16	VSS[342]
E26	VSS[243]	BC16	VSS[343]
G18	VSS[244]	BG28	VSS[344]
G20	VSS[245]	R128	VSS[345]
G26	VSS[246]		
G28	VSS[247]		
G36	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

Cougar Point/Panther Point (GND)

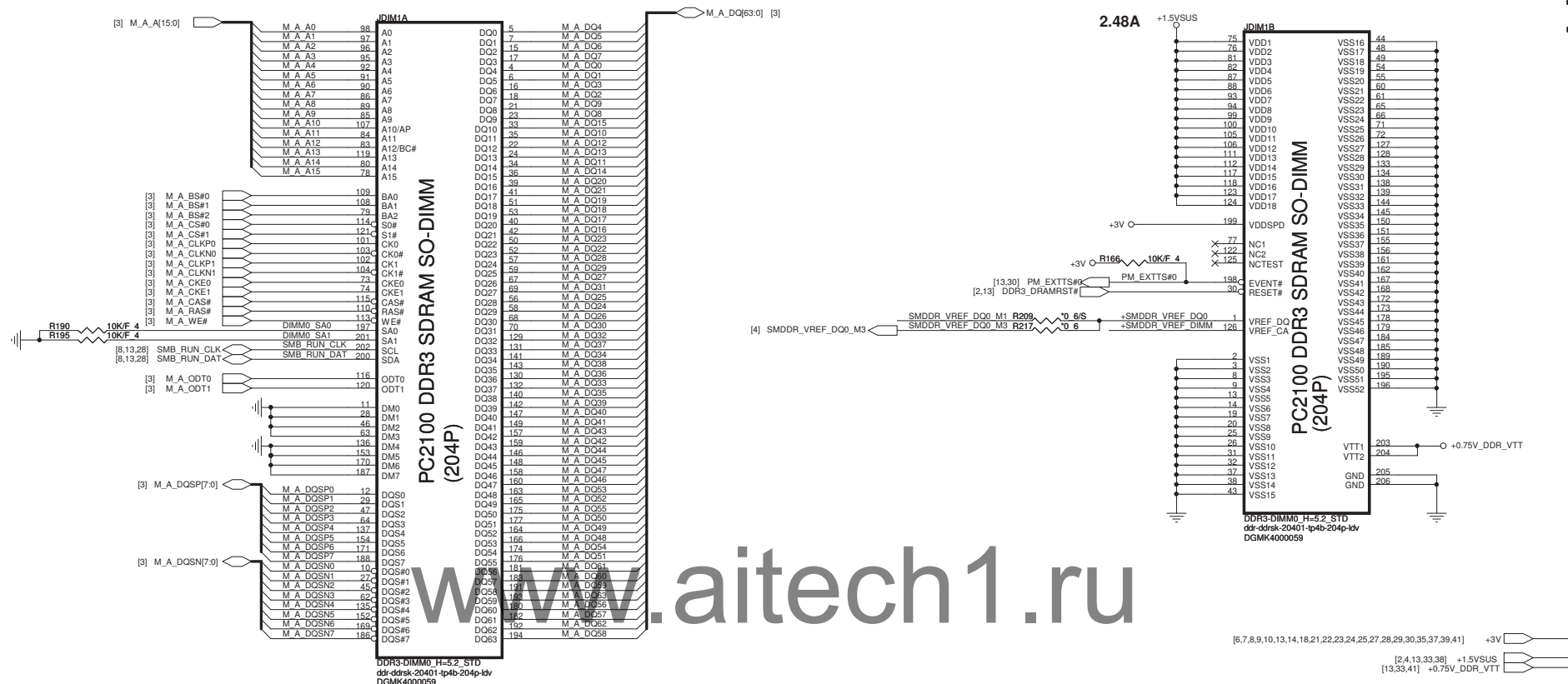
U18H
CPT_PPT_Rev_0p7

H5	VSS[0]	VSS[80]	AK38
AA17	VSS[1]	VSS[81]	AK4
AA2	VSS[2]	VSS[82]	AK42
AA3	VSS[3]	VSS[83]	AK46
AA33	VSS[4]	VSS[84]	AK6
AA34	VSS[5]	VSS[85]	AL16
AB11	VSS[6]	VSS[86]	AL17
AB14	VSS[7]	VSS[87]	AL19
AB39	VSS[8]	VSS[88]	AL2
AB4	VSS[9]	VSS[89]	AL21
AB43	VSS[10]	VSS[90]	AL23
AB5	VSS[11]	VSS[91]	AL26
AB7	VSS[12]	VSS[92]	AL27
AC19	VSS[13]	VSS[93]	AL31
AC2	VSS[14]	VSS[94]	AL33
AC21	VSS[15]	VSS[95]	AL34
AC24	VSS[16]	VSS[96]	AL48
AC33	VSS[17]	VSS[97]	AM11
AC34	VSS[18]	VSS[98]	AM14
AD10	VSS[19]	VSS[99]	AM36
AD11	VSS[20]	VSS[100]	AM39
AD12	VSS[21]	VSS[101]	AM43
AD13	VSS[22]	VSS[102]	AM45
AD19	VSS[23]	VSS[103]	AM46
AD24	VSS[24]	VSS[104]	AM7
P11	VSS[25]	VSS[105]	AN2
AD27	VSS[26]	VSS[106]	AN29
AD33	VSS[27]	VSS[107]	AN3
AD34	VSS[28]	VSS[108]	AN31
AD36	VSS[29]	VSS[109]	AP12
AD37	VSS[30]	VSS[110]	AP19
AD38	VSS[31]	VSS[111]	AP28
AD39	VSS[32]	VSS[112]	AP28
AD4	VSS[33]	VSS[113]	AP32
AD40	VSS[34]	VSS[114]	AP38
AD42	VSS[35]	VSS[115]	AP4
AD43	VSS[36]	VSS[116]	AP42
AD45	VSS[37]	VSS[117]	AP46
AD46	VSS[38]	VSS[118]	AP8
AD8	VSS[39]	VSS[119]	AP2
AE2	VSS[40]	VSS[120]	AB48
AE3	VSS[41]	VSS[121]	AT11
AE10	VSS[42]	VSS[122]	AT13
AE12	VSS[43]	VSS[123]	AT16
AD14	VSS[44]	VSS[124]	AT22
AD16	VSS[45]	VSS[125]	AT26
AE16	VSS[46]	VSS[126]	AT28
AE19	VSS[47]	VSS[127]	AT30
AE24	VSS[48]	VSS[128]	AT32
AE26	VSS[49]	VSS[129]	AT34
AE27	VSS[50]	VSS[130]	AT39
AE28	VSS[51]	VSS[131]	AT42
AE3	VSS[52]	VSS[132]	AT46
AE38	VSS[53]	VSS[133]	AT4
AE4	VSS[54]	VSS[134]	AT24
AE42	VSS[55]	VSS[135]	AU30
AE46	VSS[56]	VSS[136]	AV16
AE5	VSS[57]	VSS[137]	AV20
AE7	VSS[58]	VSS[138]	AV24
AE8	VSS[59]	VSS[139]	AV30
AG19	VSS[60]	VSS[140]	AV38
AG2	VSS[61]	VSS[141]	AV4
AG31	VSS[62]	VSS[142]	AV43
AG48	VSS[63]	VSS[143]	AV8
AH11	VSS[64]	VSS[144]	AW14
AH3	VSS[65]	VSS[145]	AW18
AH36	VSS[66]	VSS[146]	AW2
AH39	VSS[67]	VSS[147]	AW22
AH40	VSS[68]	VSS[148]	AW28
AH42	VSS[69]	VSS[149]	AW28
AH46	VSS[70]	VSS[150]	AW32
AH7	VSS[71]	VSS[151]	AW34
A19	VSS[72]	VSS[152]	AW36
A121	VSS[73]	VSS[153]	AW40
A124	VSS[74]	VSS[154]	AW48
A133	VSS[75]	VSS[155]	AV11
A134	VSS[76]	VSS[156]	AY12
AK12	VSS[77]	VSS[157]	AY22
AK3	VSS[78]	VSS[158]	AY28
AP1	VSS[79]		

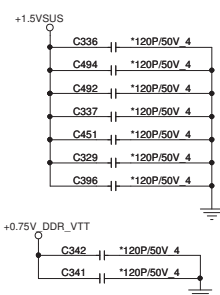


PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

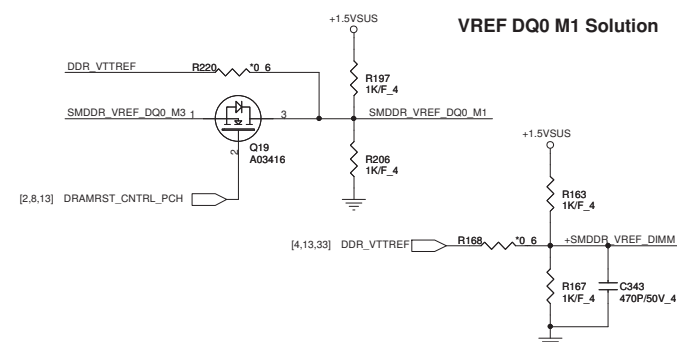
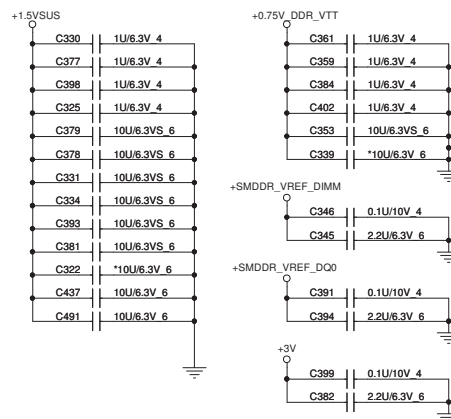
Size Custom	Document Number PCH 6/6 (Ground)	Rev A
Date: Tuesday, March 27, 2012	Sheet 11 of 42	



For EMI RESERVE 8/30

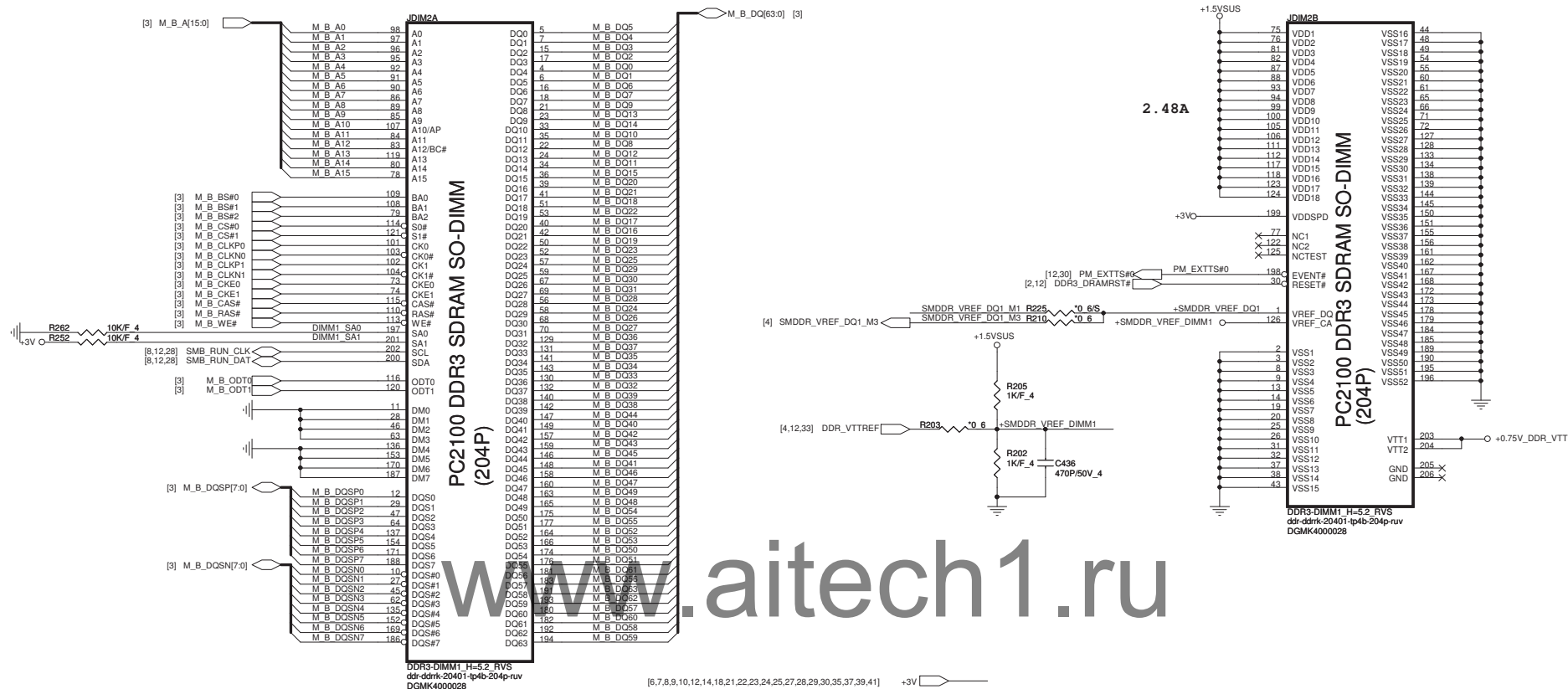


Place these Caps near So-Dimm0.



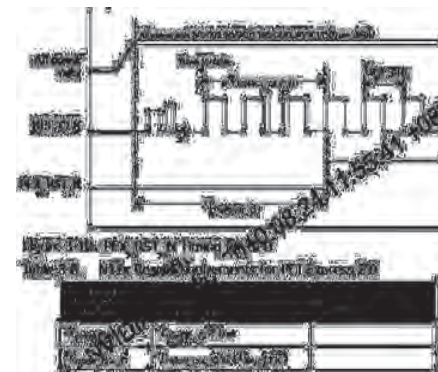
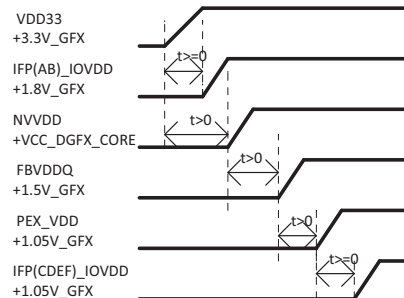
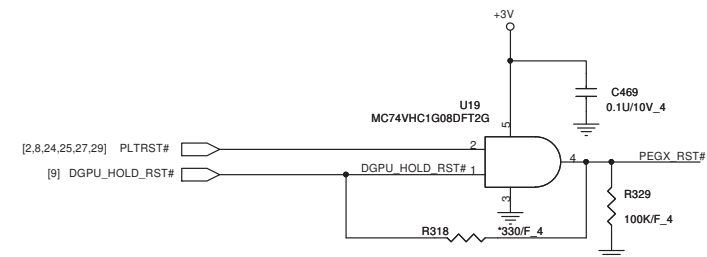
PROJECT :JW3/4 (Chief River)
 Quanta Computer Inc.

Size Custom
 Document Number
 System Memory 1/2 (5.2H)
 Date: Tuesday, March 27, 2012
 Sheet 12 of 42



PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

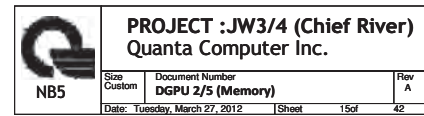
Size Custom	Document Number System Memory 2/2 (9.2H)	Rev A
Date: Tuesday, March 27, 2012	Sheet 13 of 42	



Timing diagram for PEX_RST signal. The diagram shows the I/O 3.3V supply and the PEX_RST signal. The PEX_RST signal is active-low. The rise time (T_{rise}) is marked as $\geq 1\mu s$ and the fall time (T_{fall}) is marked as $\leq 500ns$.



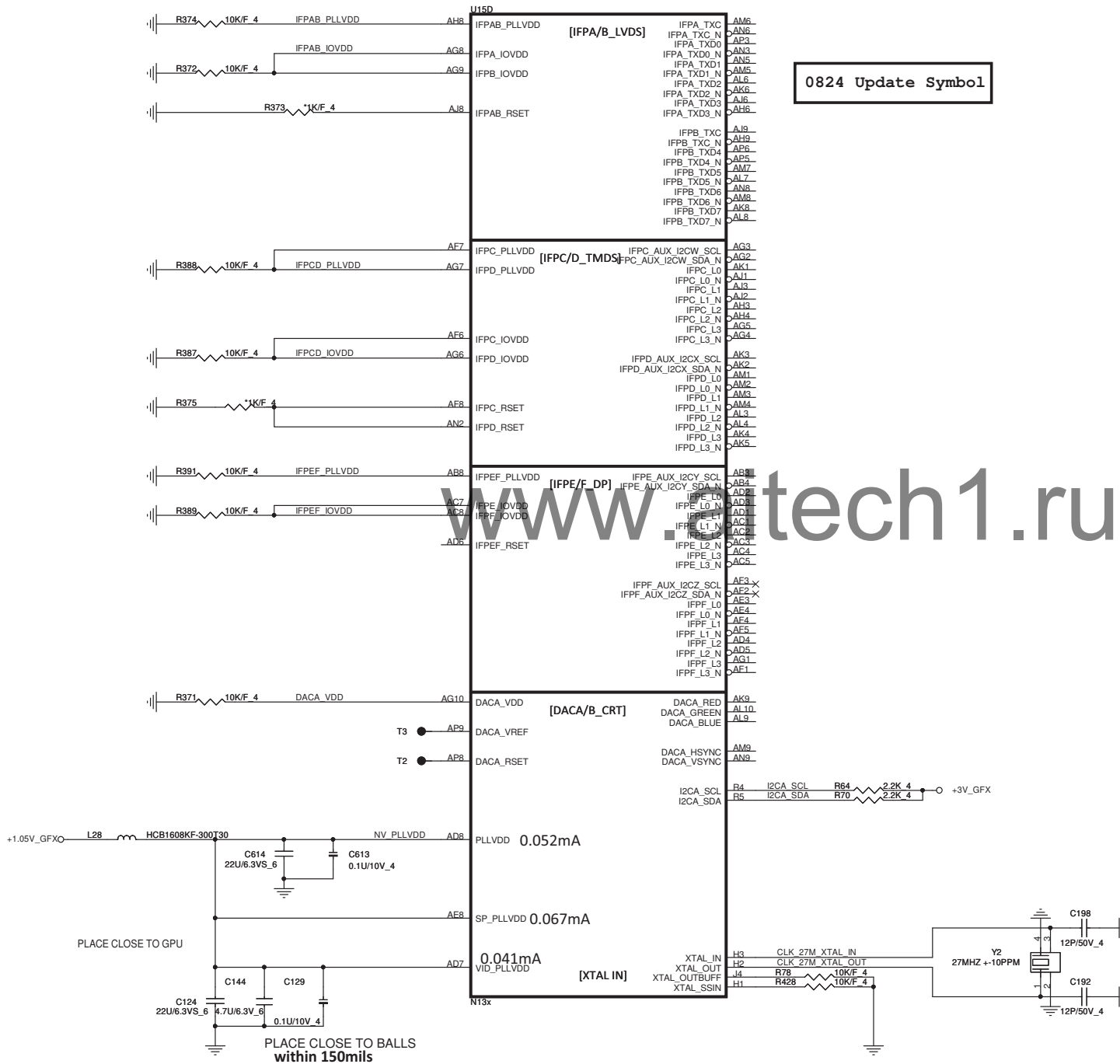
Size A3	Document Number DGPU 1/5 (PEG)	Rev A
Date: Tuesday, March 27, 2012	Sheet 14 of	42



[14,15,18,38] +1.05V_GFX
[14,17,18,37,38] +3V_GFX

0824 Update Symbol

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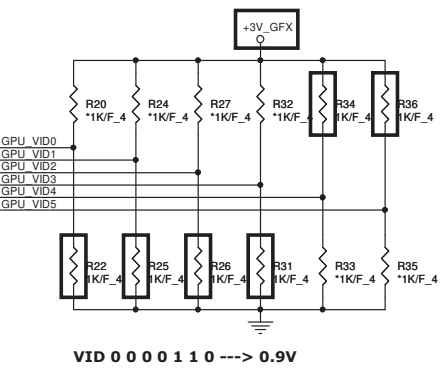
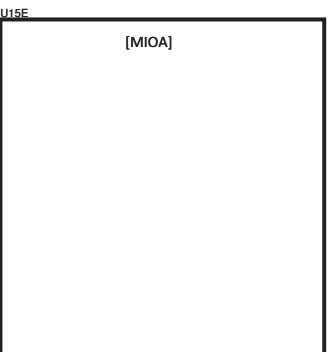
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size A3	Document Number DGPU 3/5 (Display)	Rev A
Date: Tuesday, March 27, 2012		Sheet 16 of 42

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

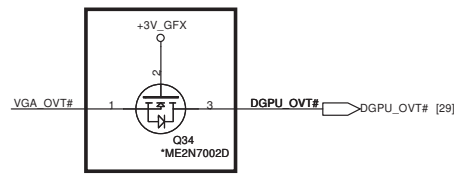
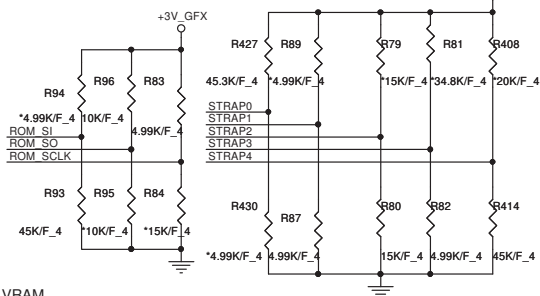
N13M-GE2-A1 ID: 0X0DEA
N13P-GS ID: 0X0FD2

Net name	N13M-GE2	N13P-GS (QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K



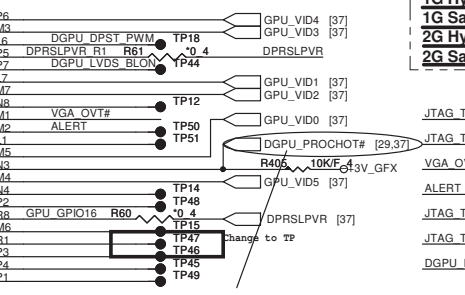
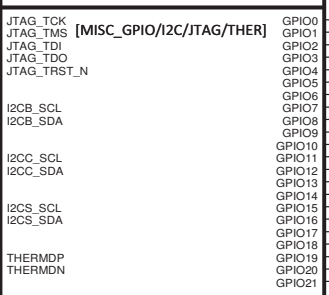
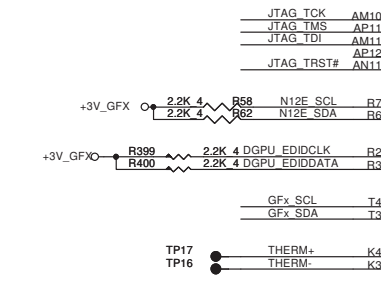
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

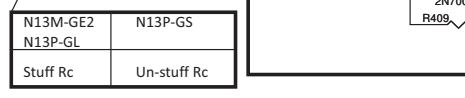
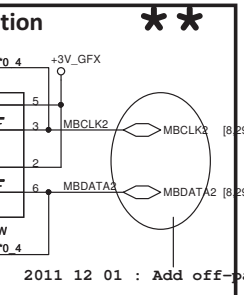
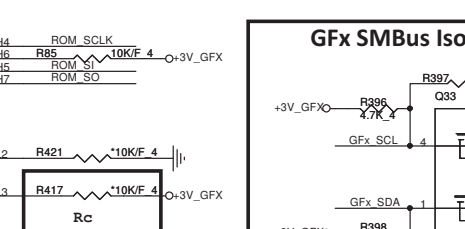
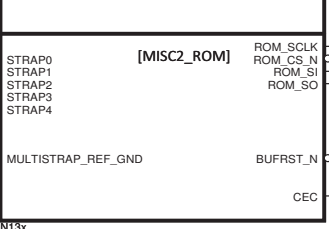
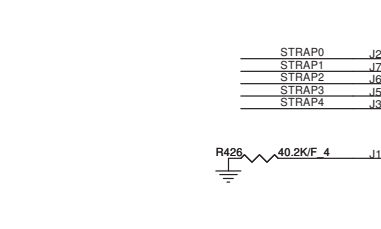
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR2_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX



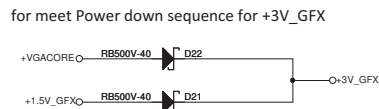
For N13M-GE2, N13M-GS (QS)
Default: 2G Samsung
VRAM Configuration Table
ROM_SI -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	



PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.
Size Custom Document Number DGPU 4/5 (MIO/GPIO) Rev A
Date: Tuesday, March 27, 2012 Sheet 17 of 42

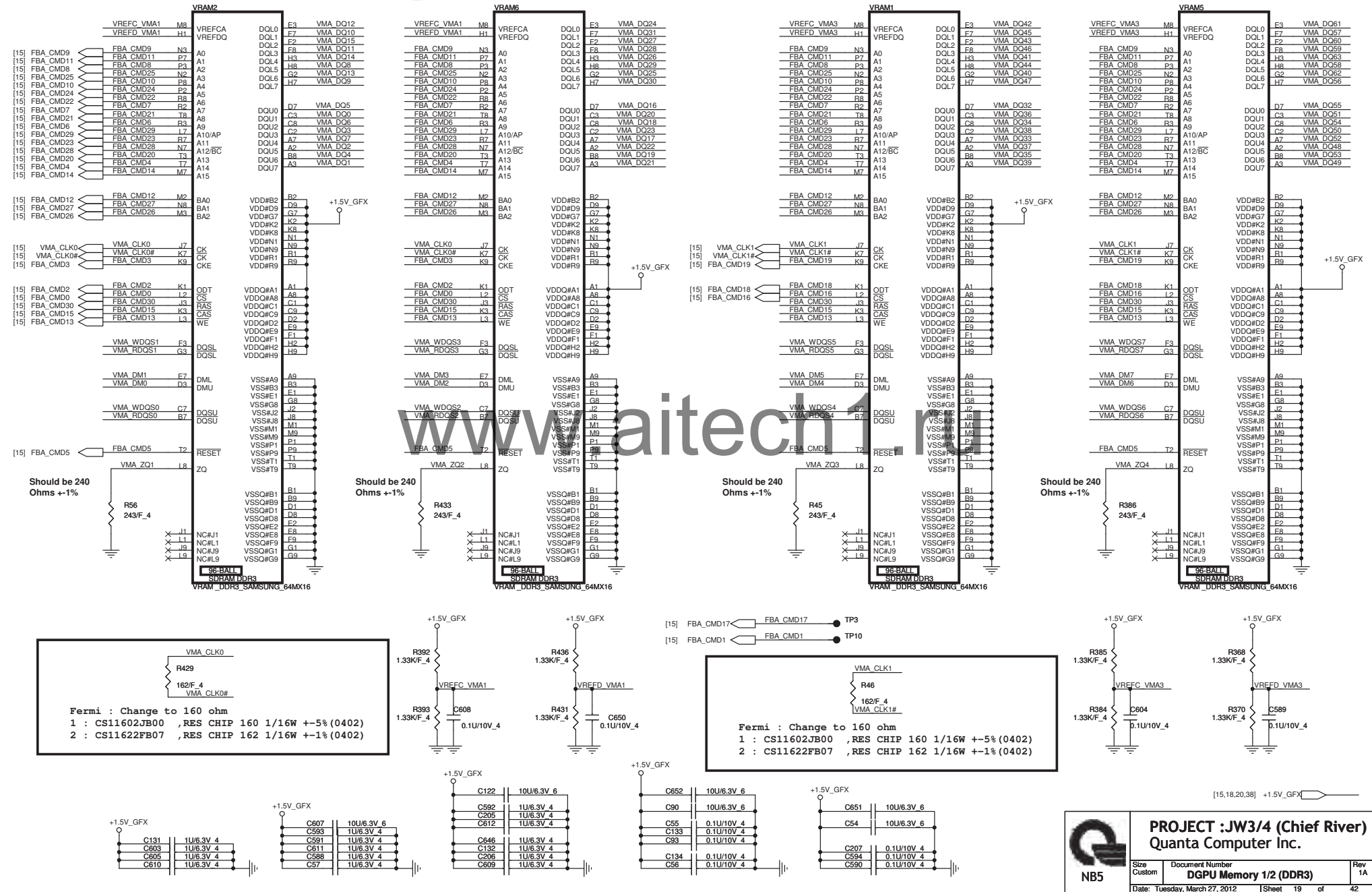


PLACE NEAR GPU



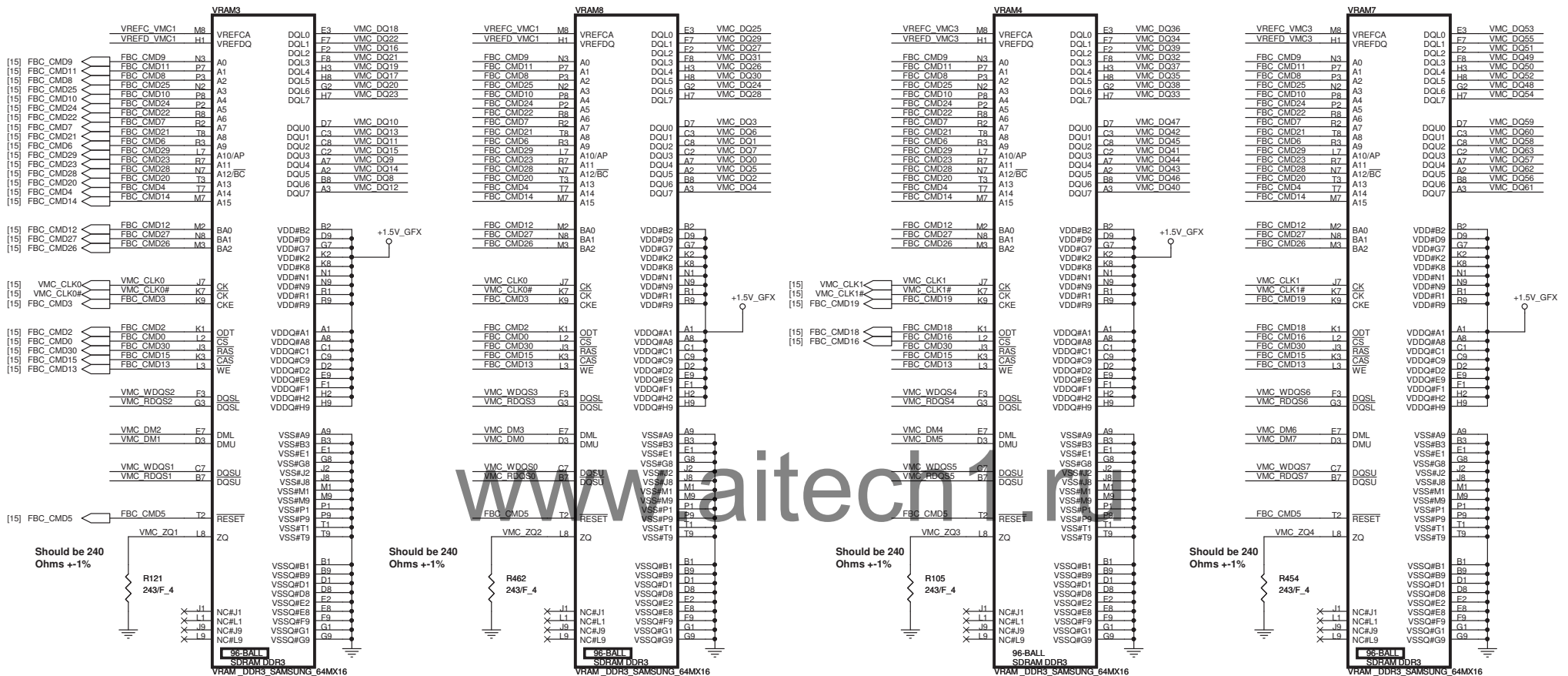
900MHz VRAM size:
 Samsung 64Mx16, P/N = AKD5EGGT500
 Samsung 128Mx16, P/N = AKD5MGWT500
 Hynix 64Mx16, P/N = AKD5LZWTW02
 Hynix 128Mx16, P/N = AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3



[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WQS[7..0]
[15] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3



Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

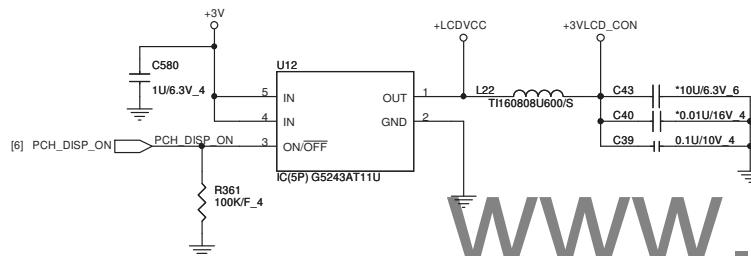
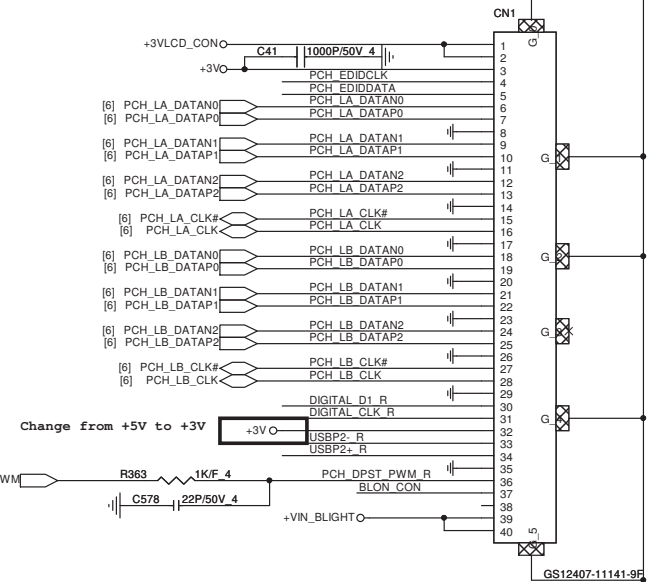
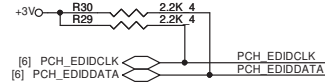
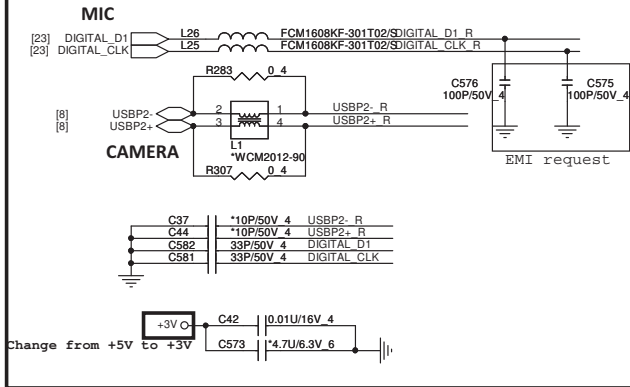
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

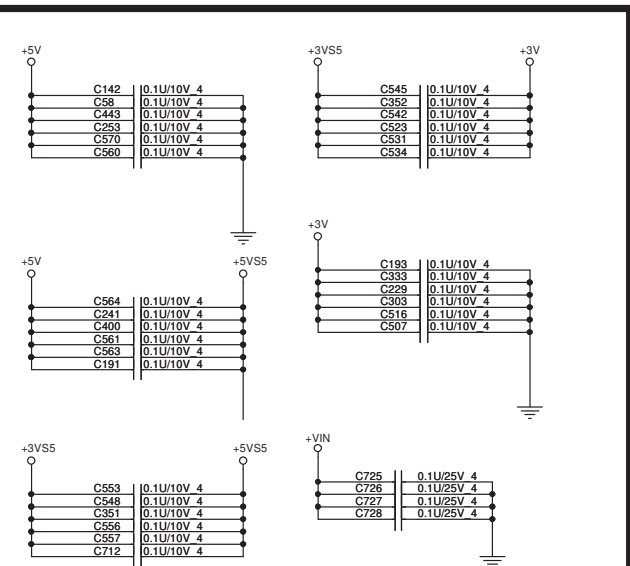


Size Custom Document Number DGPU Memory 2/2 (DDR3) Rev 1A
Date: Tuesday, March 27, 2012 Sheet 20 of 42

USB Camera Connector

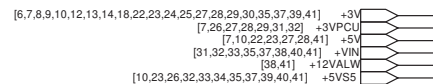
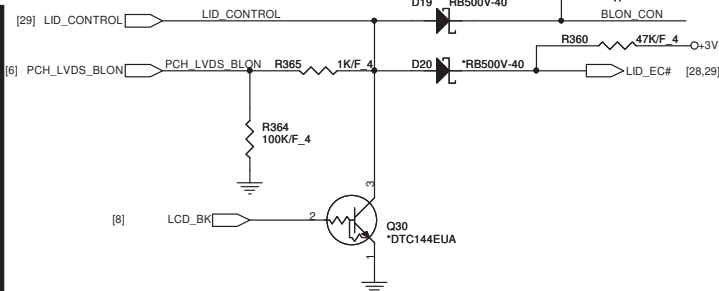


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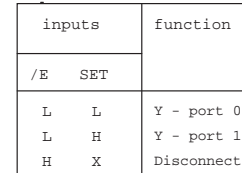


EMI/ESD

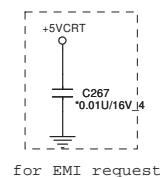
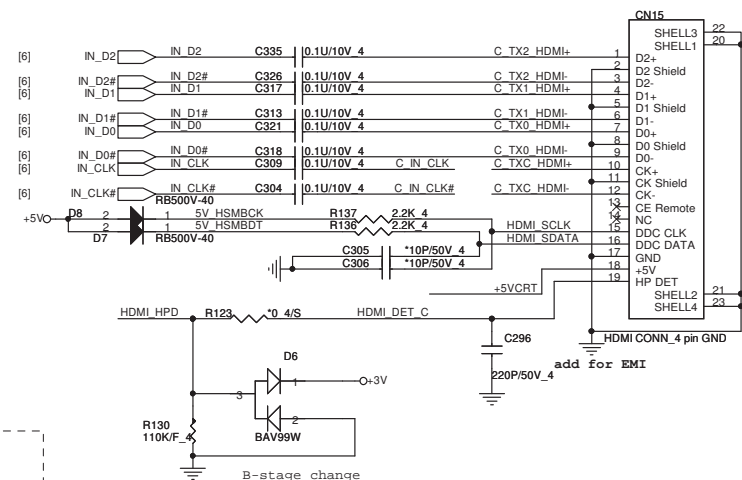
Stitching Cap(each 1" place one cap)

PROJECT : JW3/4 (Chief River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A
Date: Tuesday, March 27, 2012	Sheet 21 of 42	



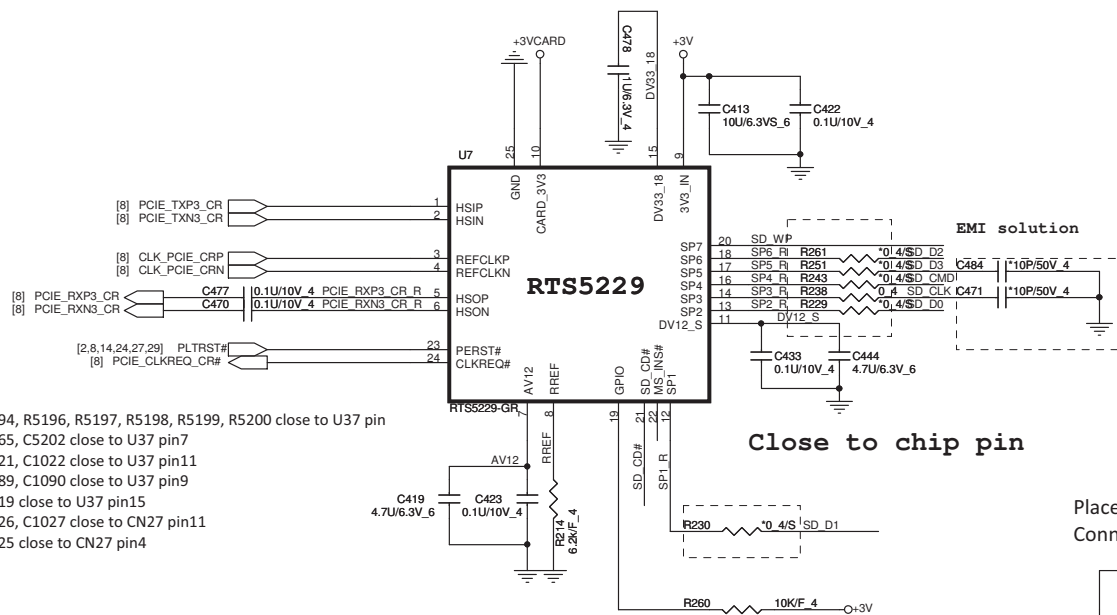
HDMI PORT



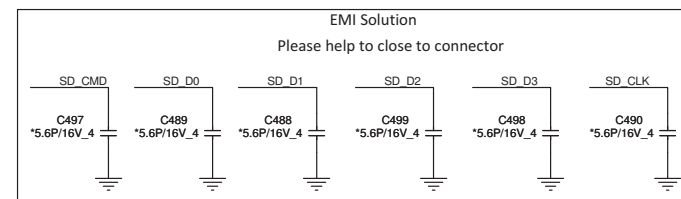
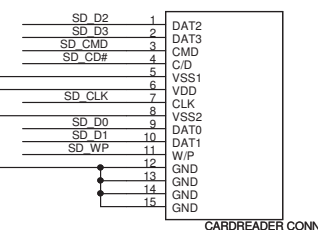
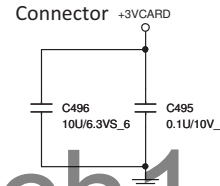
Size Custom	Document Number CRT/HDMI Connector	Rev A
Date: Tuesday, March 27, 2012	Sheet 22 of	42



Size Custom	Document Number Audio Codec (Realtek_ALC269Q-VC2-GR)	Rev A
Date: Tuesday, March 27, 2012	Sheet 23 of 42	

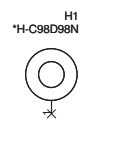
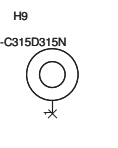
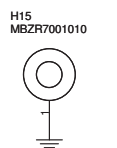
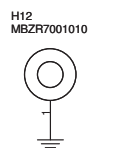
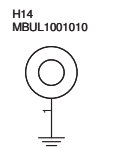
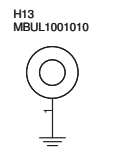
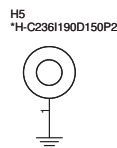
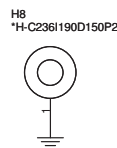
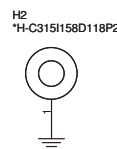
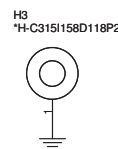
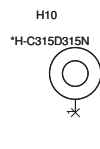
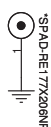
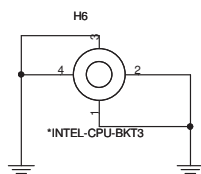
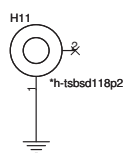


Share Pin

SD / MMC
CARD READERPlace close to
Connector

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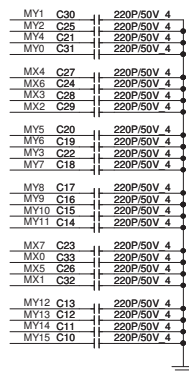
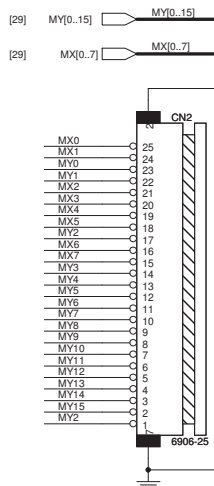
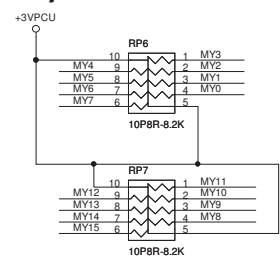
CPU Bracket

PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

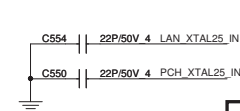
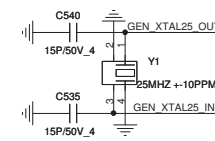
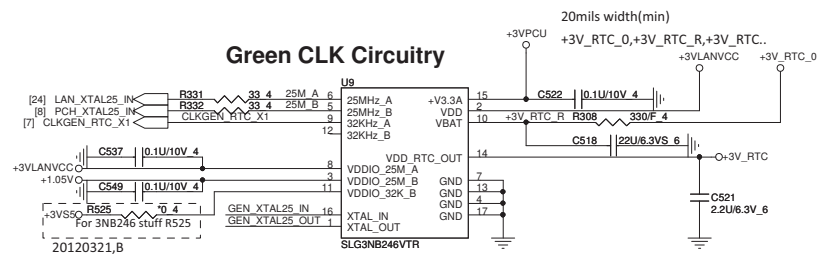
Size	Document Number	Rev
Custom	Card Reader control (RT55229-GR)	A

Date: Tuesday, March 27, 2012 Sheet 25of 42

Keyboard Connector



Green CLK Circuitry

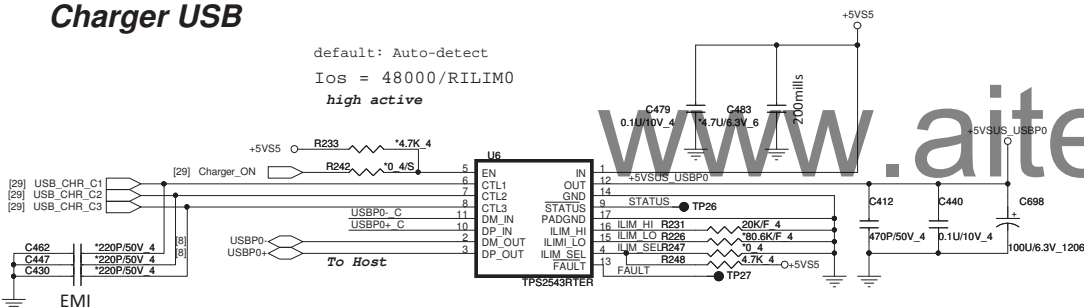


FOR TPM option

	TPM	Non-TPM
R419	Stuff	NA
U5	AL3NB246000	AL3NB244000

Charger USB

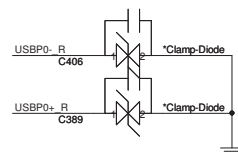
default: Auto-detect
Ios = 48000/RILIM0
high active



TPS2543/45 Control Truth Table

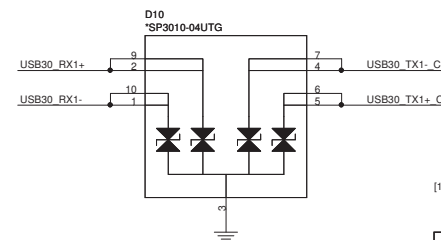
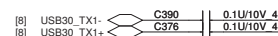
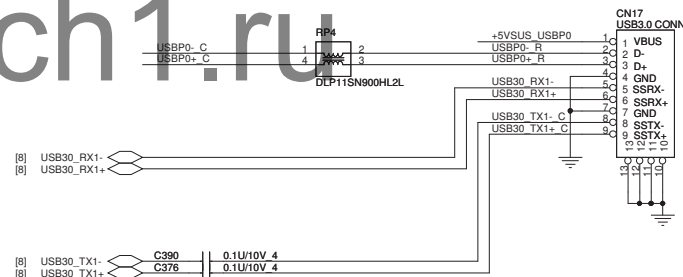
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R5233), 2.4A



USB3.0 X 1/USB2.0 COMBO

USB 3.0



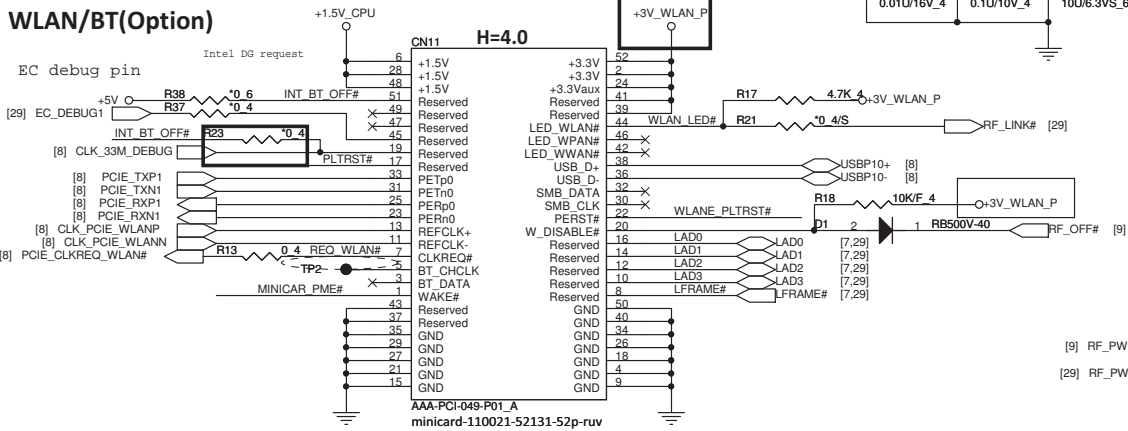
[10,21,23,32,33,34,35,37,39,40,41] +5VS5
[7,21,27,28,29,31,32] +3VPCU



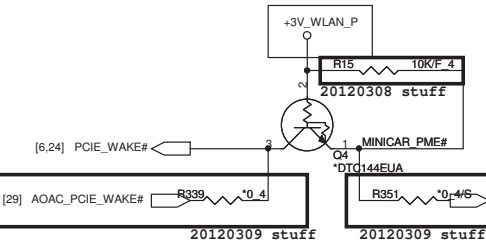
PROJECT :JW3/4 (Chief River)
Quanta Computer Inc.

Size Custom Document Number **USB 3.0/KB/Green CLK** Rev A
Date: Tuesday, March 27, 2012 Sheet 26 of 42

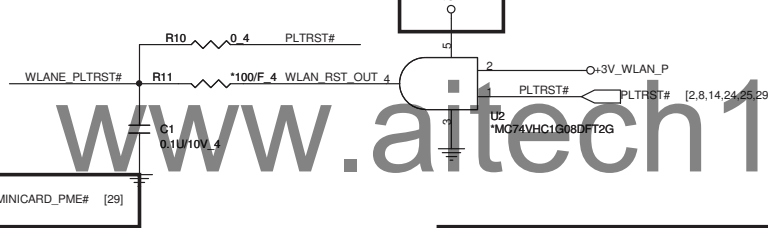
**Mini Card
WLAN/BT(Optional)**



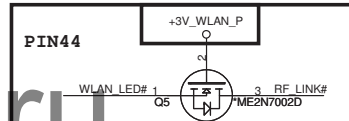
Support Wake Function(Reserve)



Mini Card Reset



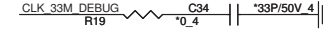
Avoid leakage issue



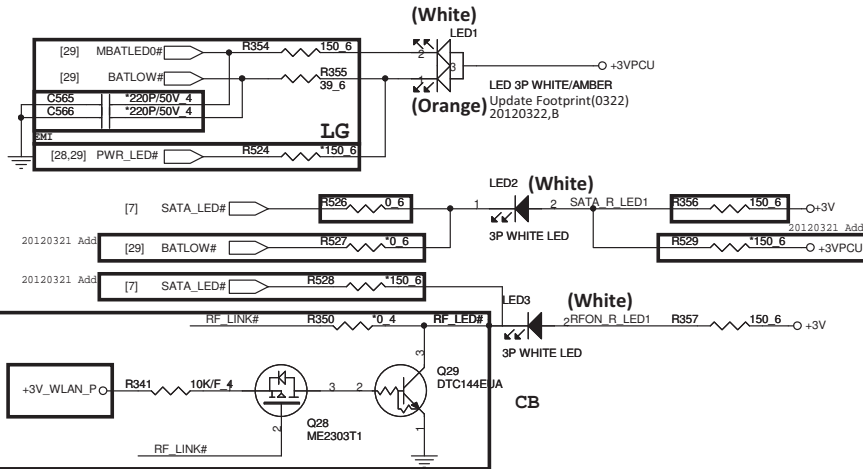
```
LGE mini-pcie power status
```

WLAN	Bluetooth	+3V WLAN
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

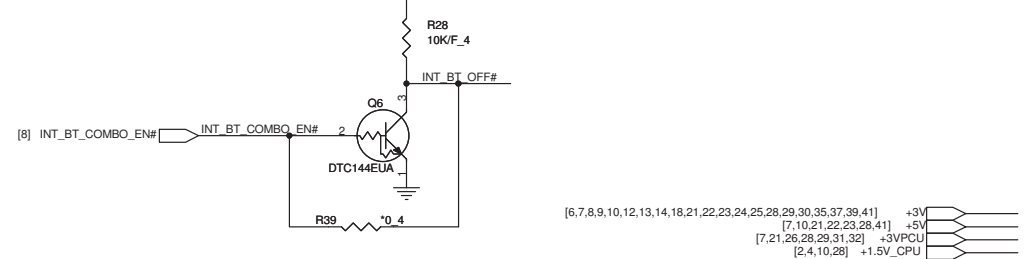
For EMI Suggestion



LED Status



PIN19, 51



9/4 Intel COMBO card control circuit

- 1.add R1001,R1002,Q1001
- 2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

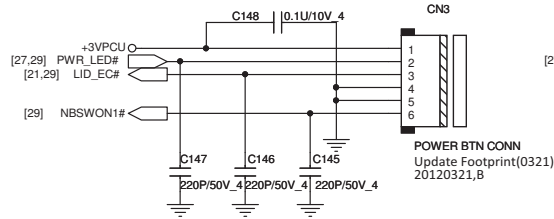


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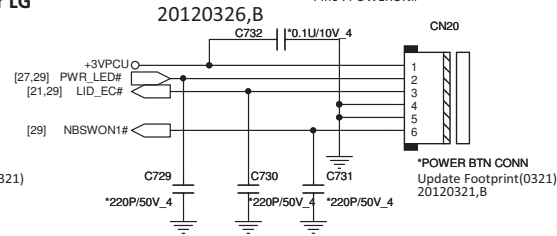
Left side Power Button Connector For CB

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

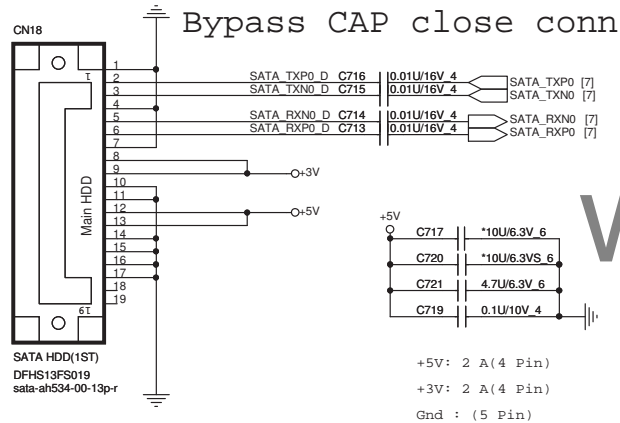


Right side Power Button Connector(2) For LG

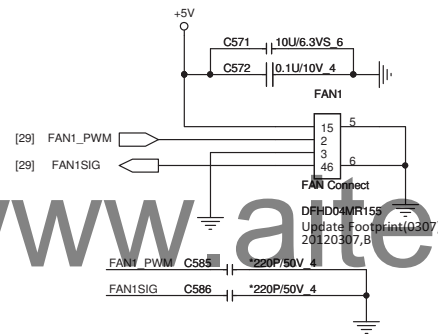
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



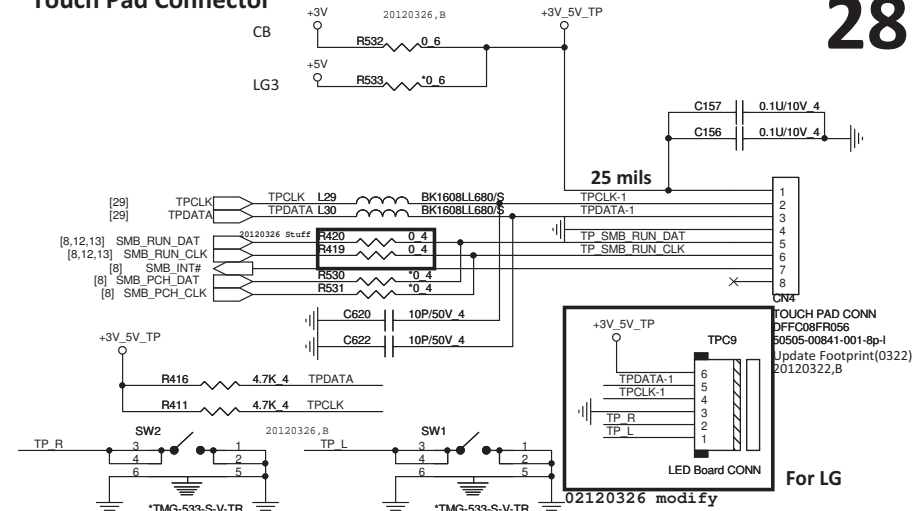
SATA HDD Connector(Cable type)



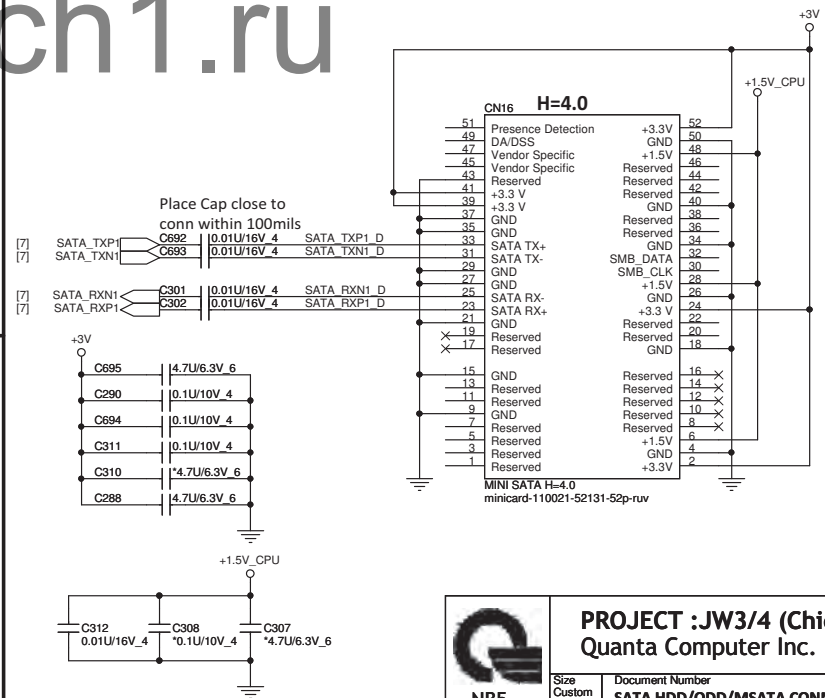
CPU FAN



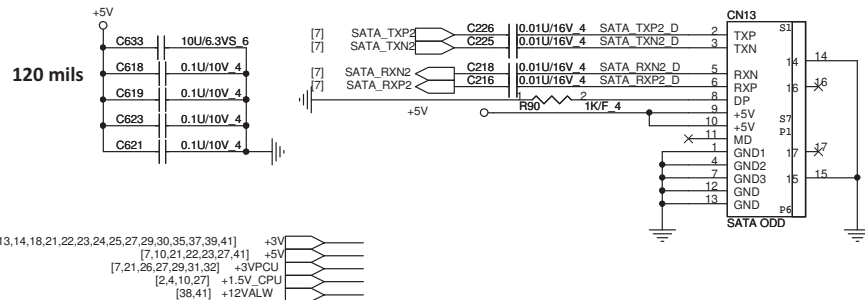
Touch Pad Connector



Mini PCI-E Card 2- Full size MINISATA

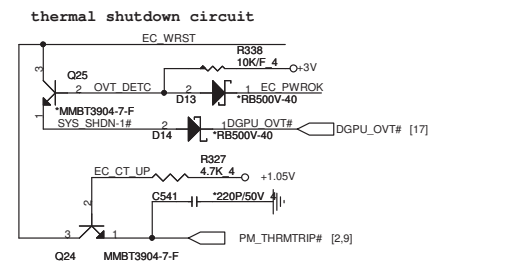
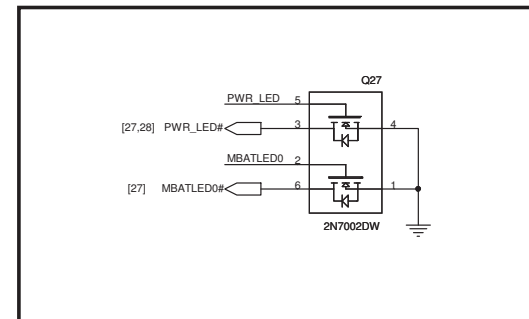
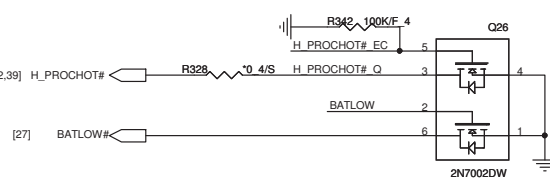


SATA ODD Connector



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Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	A
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Socket: DG008000031

U11

EC CE#	47	4	EC SCK	1	CE#	VDD	8
EC SCK R349	47	4	EC SCK	1	CE# <th>SCK</th> <th>7</th>	SCK	7
EC SCK R353	47	4	EC SI	8	SI <th>SO</th> <th>4</th>	SO	4
EC SO R344	15	4	EC SI R	2	HOLD# <th></th> <th></th>		
					WP# <th>VSS</th> <th>4</th>	VSS	4

+3VPCUO R352 10K/F 4 3

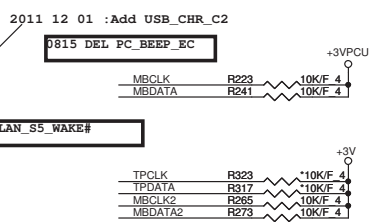
R345 10K/F 4 7

C559 0.1U/10V 4

+3VPCU

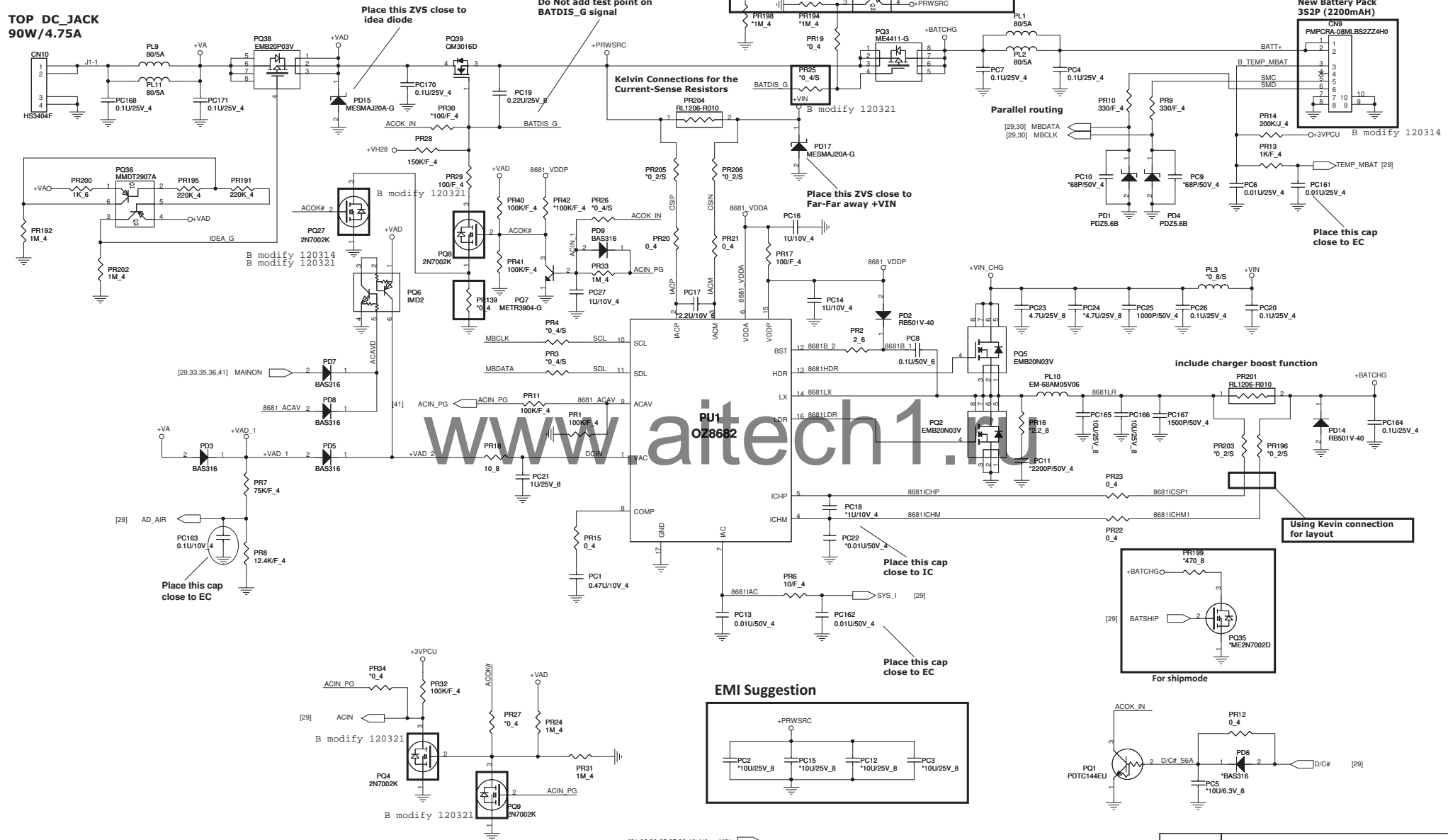


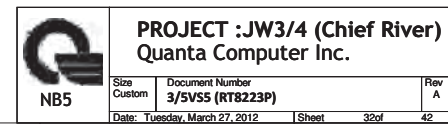
Size Custom	Document Number Embedded Controller (ITE_IT8518)	Rev A
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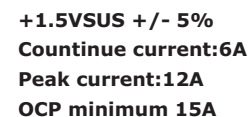


Platform	ADC
JW6/7	0V
Reserve	0.75V
Reserve	1.5V
Reserve	2.25V
JW3	3V

TOP DC JACK 90W/4.75A







**Place this short pad
close to output CAP**

Place this FB parts close to IC

[21,31,32,35,37,38,40,41]	+VIN	
[10,21,23,26,32,34,35,37,39,40,41]	+5VS5	
[2,4,12,13,38]	+1.5VSUS	
[12,13,41]	+0.75V_DDR VTT	



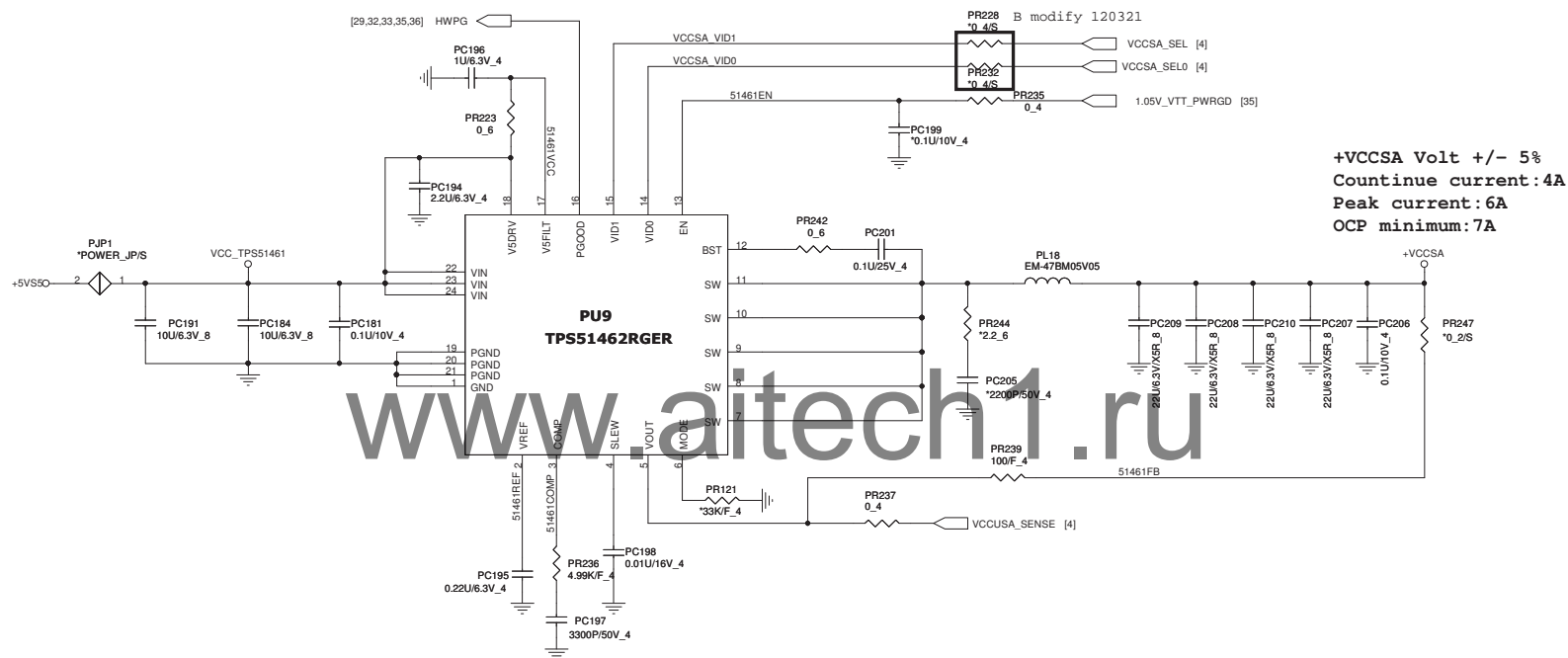
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Quanta Computer Inc.

Size Custom	Document Number DDR3 (RT8207)	Rev A
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TPS51462RGER for SV CPU

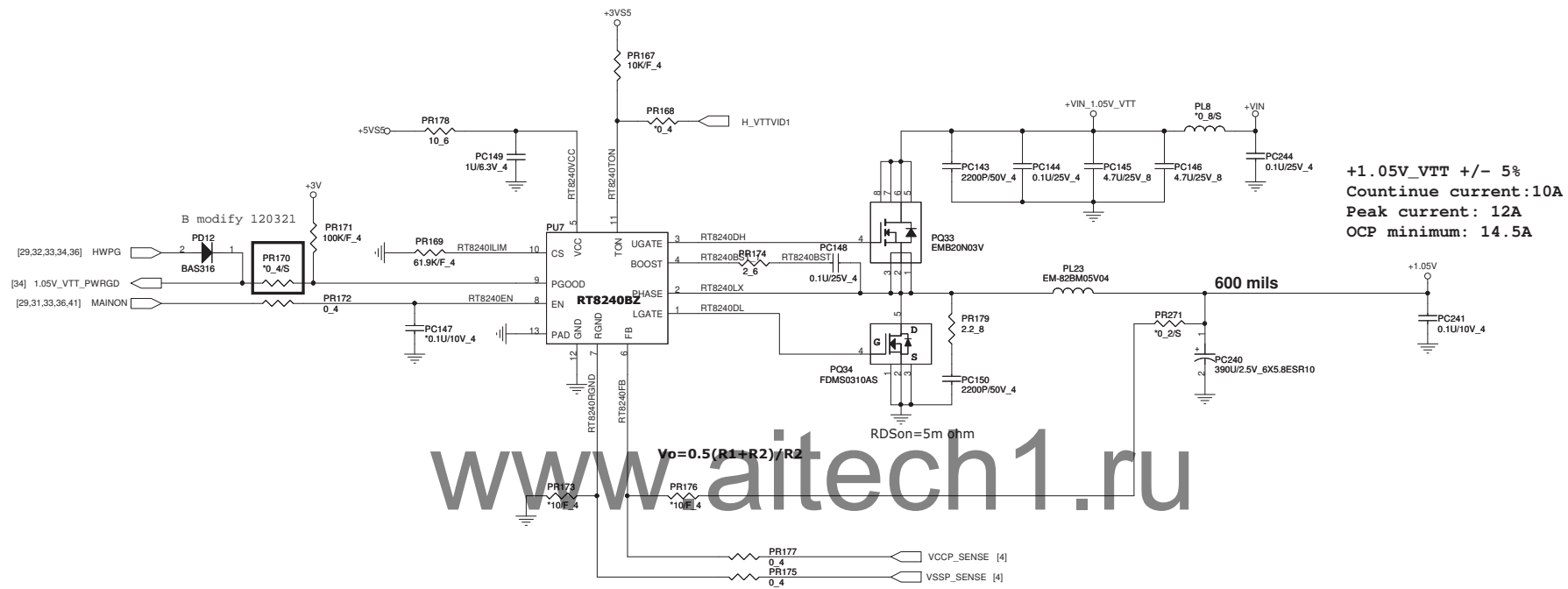
CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

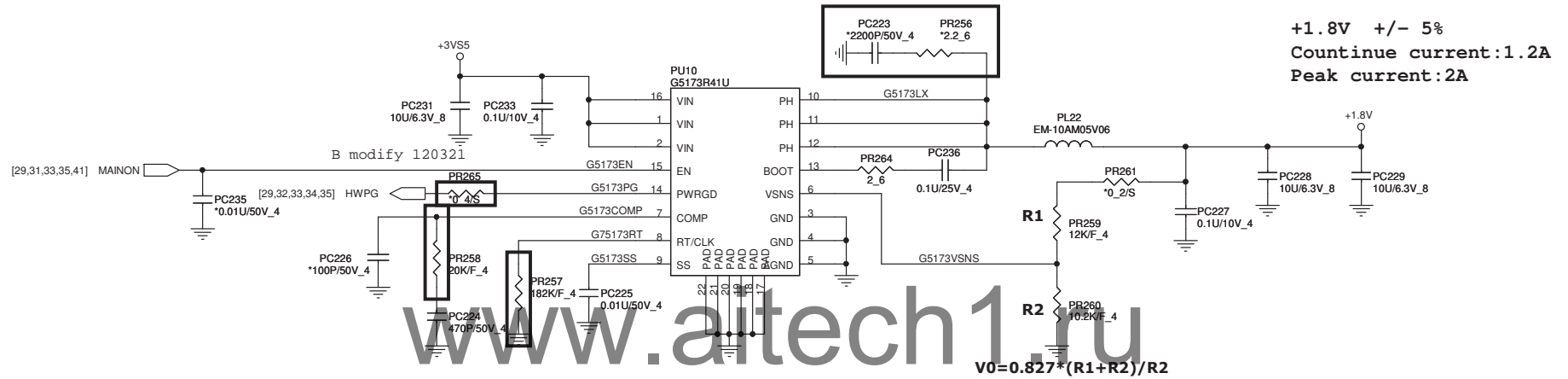
SELO	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



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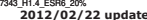
Size	Document Number	Rev
Custom	+VCCSA (TPS51462RGER)	A
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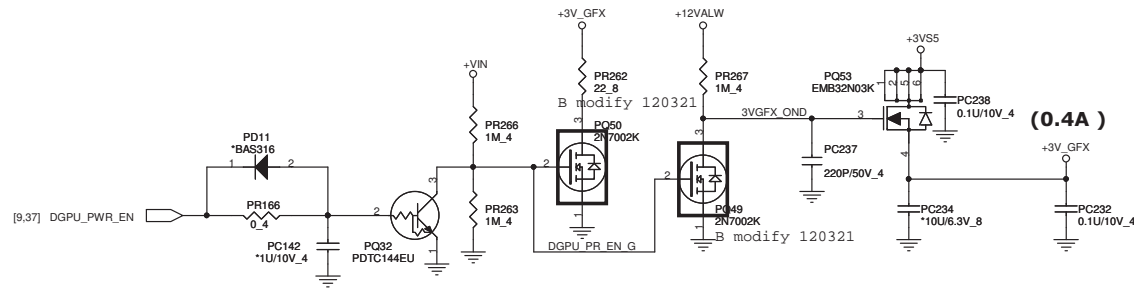


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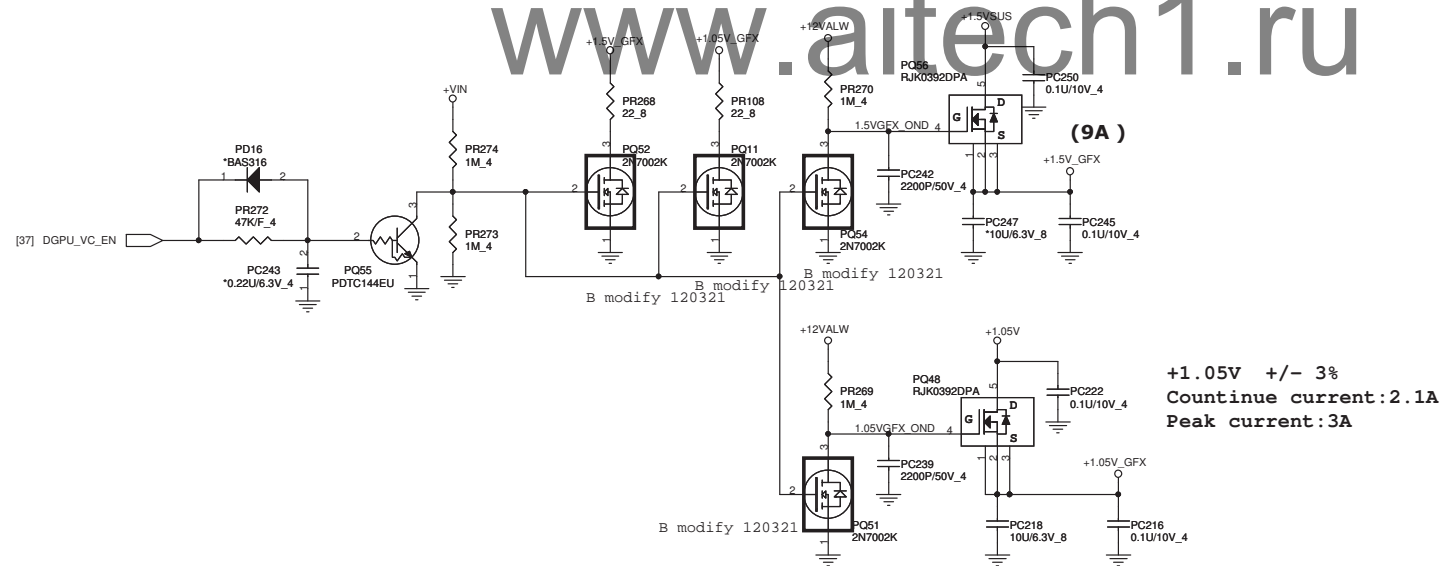
Size	Document Number	Rev
B	+1.8V (G9661)	A
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[2,4,12,13,33]	+1.5VSUS
[8,9,10,21,26,27,29,32,35,36,41]	+3VS5
[14,16,17,18,37]	+3V_GFX
[15,18,19,23]	+1.5V_GFX
[14,15,16,18]	+1.05V_GFX
[41]	+12VALW
[2,4,6,7,8,10,26,29,35,39]	+1.05V

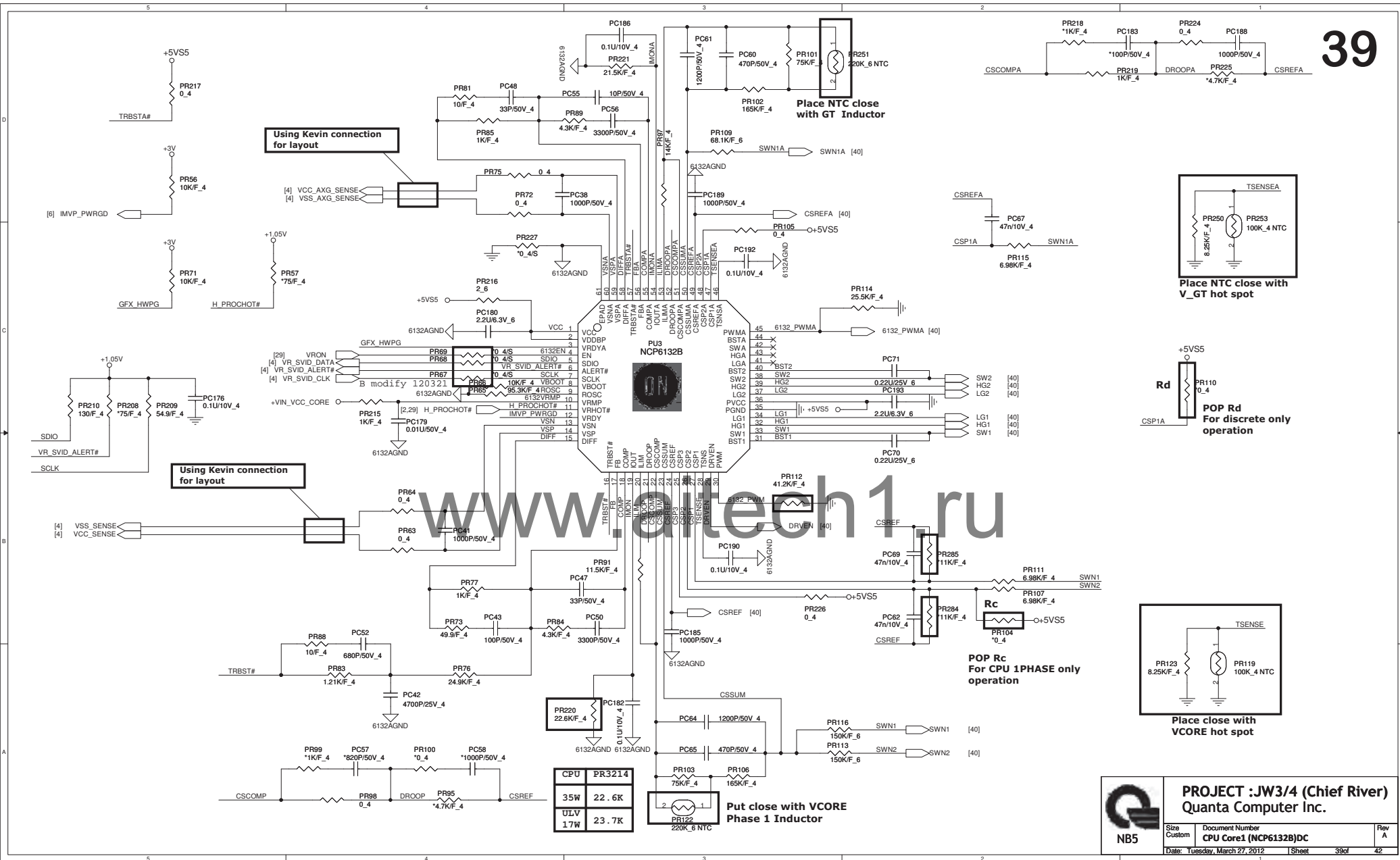


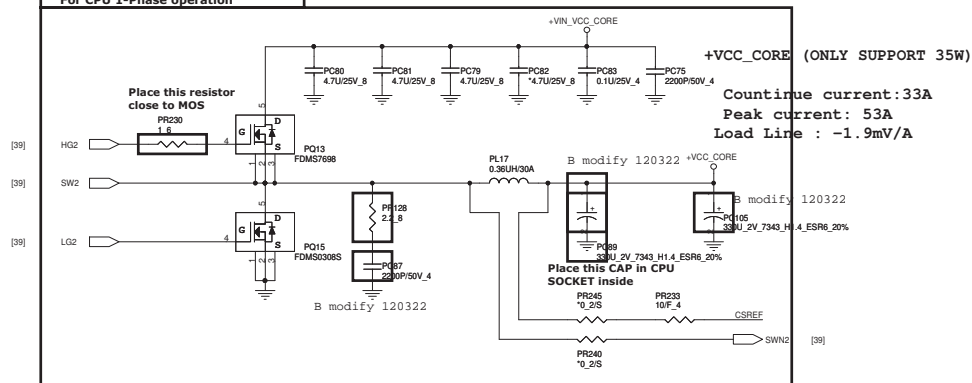
www.aitech1.ru



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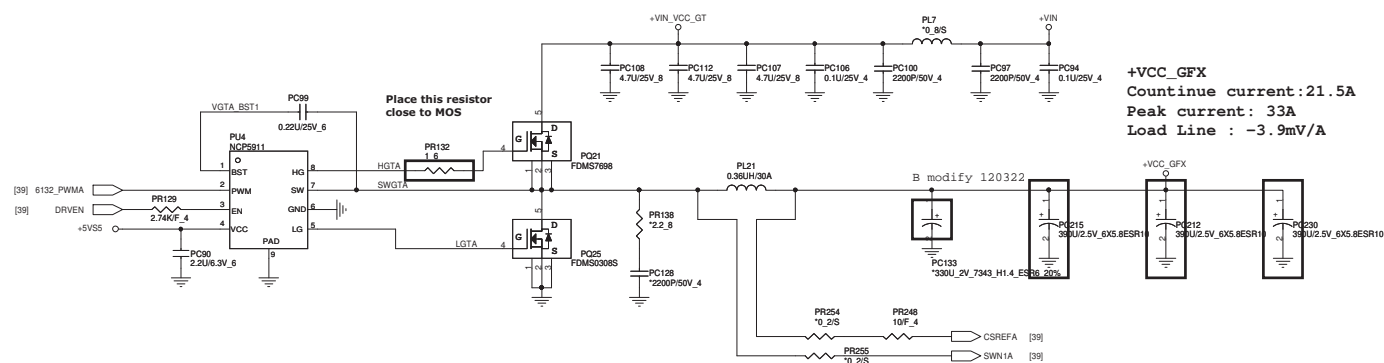
Size Custom	Document Number +VGA POWER	Rev A
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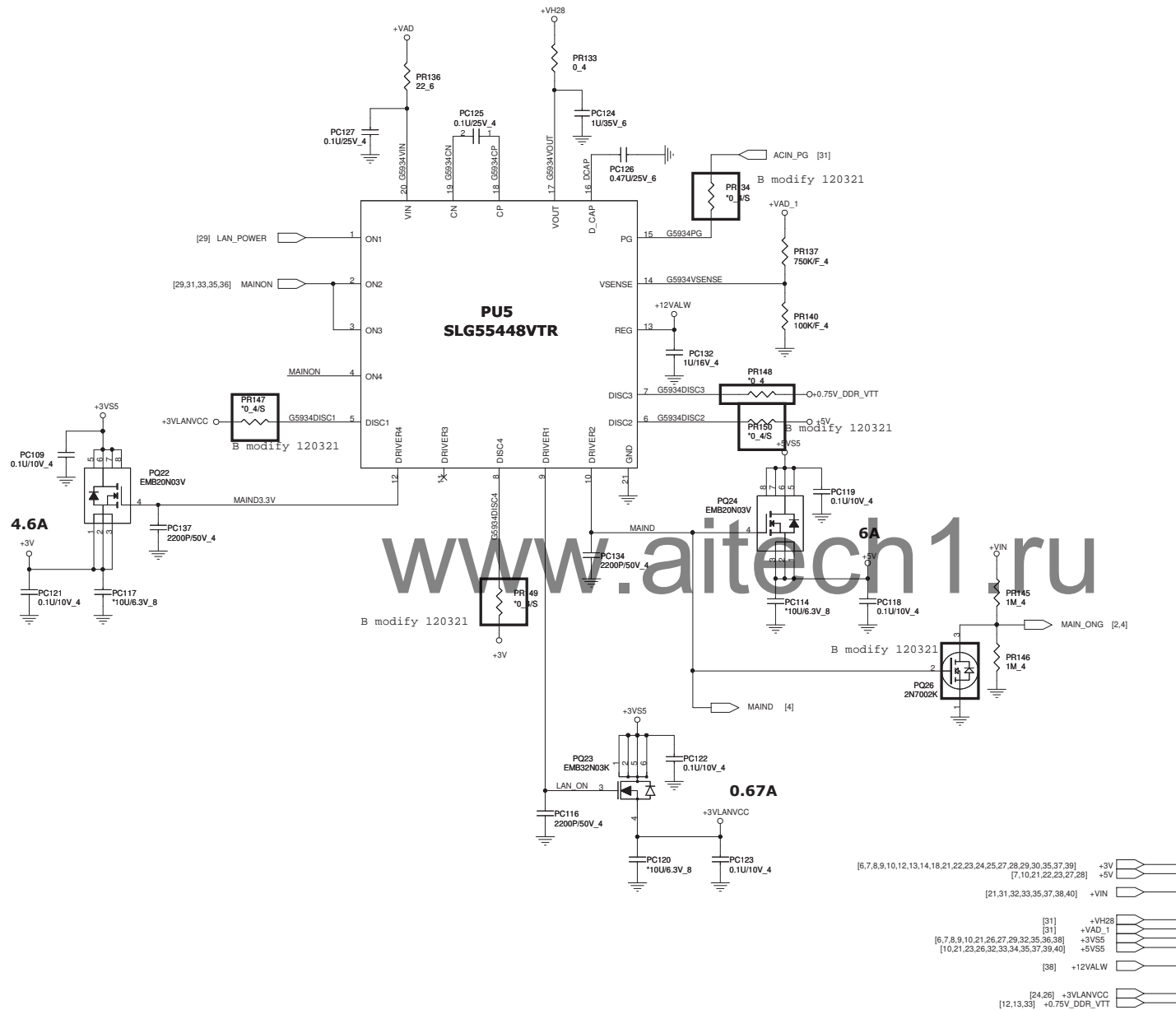


TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A

Load Line : -1.9mV/A



Size C	Document Number CPU Core2 (NCP5911)DC	Rev A
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